Electronic Version
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Claims

[c1] An apparatus that comprises the functions of a conventional random access memory of: (A) means for storing and retrieving data using addressable registers within the apparatus, (B) a plurality of external bus connections to an external bus comprising address bus, data bus and control bus, and (C) the external bus connections facilitating the means for exclusively storing or retrieving data using the addressable registers within the apparatus; wherein the improvement comprising:
(a) a command bit input,
(b) memory means for behaving as a conventional random access memory when the command bit input is negatively asserted, and
(c) instruction means for receiving instructions to the apparatus from the external bus when the command bit input is positively asserted.

[c2] An apparatus of claim 1, its instruction means further comprising:
(a) characterizing means for characterizing the content of multiple internal registers using: (A) the address bus of the external bus to send the characterizing instruction

to the apparatus, and (B) the data bus of the external bus to get the characterization result form the apparatus; and

(b) processing means for concurrently processing multiple internal registers within the apparatus using the address bus or the data bus or both of the external bus to send the processing instruction to the apparatus.

[c3] An apparatus of claim 1, further comprising termination means for signaling the termination of the instruction means by:

(a) means for changing the content of the external bus of the apparatus in a predefined way, or

(b) means for waiting a predefined time period before able to receive another input from the command bit input and the external bus connections, or

(c) the combination of (a) and (b).

[c4] Compliance means for making the connection to the external bus of the apparatus of claim 1 in full compliance with a bus standard, the compliance means comprising:

(a) means for making the apparatus' external bus connections to the data bus in full compliance with the data bus portion of the bus standard, and being connected thereof,

(b) means for making the apparatus' external bus connections to the address bus in full compliance with the

corresponding bits of the address bus portion of the bus standard, and being connected thereof,
(c) means for making the apparatus' command bit input in full compliance with a bit of the address bus of the bus standard which is not used to connect to the apparatus' connections to the address bus, as if the address bus bit of the bus standard is being used as a address bus bit, and being connected thereof, and
(d) means for making the apparatus' external bus connections to the control bus in full compliance with the bits or bits' logic combinations of the control bus portion and the remained unconnected bits of the address bus portion of the bus standard, and being connected thereof.

[c5] Preferred compliance means for the apparatus' connection to the external bus in full compliance with a bus standard as claimed in claim 4, the preferred compliance means further comprising:
(a) connecting the apparatus' command bit input with the least significant address bit of the bus standard which is not connected to the apparatus' external bus connection to the address bus.

[c6] Possible compliance means for the apparatus' connection to the external bus in full compliance with a bus standard as claimed in claim 4, the possible compliance

means further comprising:
(a) the apparatus having additional instruction bits to increase the width of instructions for the apparatus, and
(b) the instruction bits being able to be connected to the external bus.

[c7] Using steps for using the apparatus when it is connected with other devices using an external bus of a bus standard, as claimed in claim 4, the using steps comprising:
(a) negatively asserting the command bit input of the apparatus, to use the apparatus as a conventional random access memory,
(b) positively asserting the command bit input of the apparatus, and sending a processing instruction to the apparatus as if storing data to a fictional location inside the apparatus, and
(c) positively asserting the command bit input of the external bus, and sending a characterizing instruction to the apparatus as if retrieving data from a fictional location inside the apparatus.

[c8] An apparatus comprising:
(a) a plurality of memory elements, each of which comprising:
(1) at least one register;
(2) element instruction means for receiving and carrying out instructions for the memory element;

(3) an enable bit input; and

(4) disabling means for disabling the element instruction means when the enable bit input is negatively asserted;

(b) a concurrent bus, which is connected to all the memory elements, and which is concurrently read by all the enabled memory elements;

(c) an exclusive bus, which is connected to a plurality of registers, and which is exclusively read from or exclusively written to by any one of the connected registers, the connected registers being addressable registers, each having a register address;

(d) an input/output control unit, comprising:

(1) means for connecting with external bus connections of the apparatus, and means for receiving instruction from the external bus;

(2) means for connecting to the concurrent bus, and means for writing exclusively to the concurrent bus; and

(3) means for connecting to the exclusive bus, and means for either (A) exclusively writing to the exclusive bus, or (B) exclusively reading from the exclusive bus;

(e) exclusive means for exclusively copying either (A) the content of any addressable register to the exclusive bus, or (B) the content of the exclusive bus to any addressable

register, or (C) the content of a source within the input/output control unit to the exclusive bus; or (D) the content of the exclusive bus to a target within the input/output control unit.

(f) concurrent means for concurrently executing a same instruction on the concurrent bus in a plurality of the enabled memory elements, the concurrent means further comprising:

(1) instructing means for sending a instruction from the input/output control unit, through the concurrent bus, to each of all the memory elements concurrently;

(2) enabling means for positively asserting the enable bit inputs of a plurality of memory elements; and

(3) executing means for concurrently executing the instruction in each of all the enabled memory elements; and

(g) instruction means for receiving and carrying out instructions at the external bus connections of the apparatus.

[c9] An apparatus of claim 8, its instruction means further comprising:

(a) means for signaling the values of all the outputs of the apparatus being invalid for the current input values;

(b) means for translating the content of the external bus

of the apparatus into instructions for the apparatus; and (c) means for carrying out the instruction for the apparatus in a series of steps comprising the concurrent means and the exclusive means.

[c10] An apparatus of claim 8 that comprises the functions of a conventional random access memory of: (A) means for storing and retrieving data using addressable registers within the apparatus, (B) a plurality of external bus connections to an external bus comprising address bus, data bus and control bus, and (C) the external bus connections facilitating the means for exclusively storing or retrieving data using the addressable registers within the apparatus; wherein the improvement comprising:

(a) a command bit input,

(b) the external bus connections of the input/output control unit further comprising address bus, data bus and control bus;

(c) memory means for behaving as a conventional random access memory containing a plurality of addressable register which is exclusively addressable and accessible through the external bus connections of the apparatus when the command bit input is negatively asserted, the memory means further comprising:

(1) storing means for copying the content of the data bus of the external bus to the addressable register

whose register address is specified by the address bus of the external bus when the control bus of the external bus instructs the apparatus for a storing operation; and

(2) retrieving means for copying the content of the addressable register whose register address is specified by the address bus of the external bus to the data bus of the external bus when the control bus of the external bus instructs the apparatus for a retrieving operation;.

(d) the instruction means further comprising means for receiving and carrying out instructions for the apparatus when the command bit input is positively asserted.

[c11] An apparatus of claim 10, its instruction means further comprising:

(a) means for signaling the values of all the outputs of the apparatus being invalid for the current input values;

(b) means for translating the content of the external bus of the apparatus into instructions for the apparatus when the command bit input is positively asserted; and

(c) means for carrying out the instruction for the apparatus in a series of steps comprising the concurrent means and the exclusive means; and

(d) means for using an existing bus standard protocol to signal the readiness of the apparatus.

[c12] An apparatus of claim 8, further comprising:

(a) a plurality of bit storage elements;

(b) means for connecting:

(1) each enable bit input of all the memory elements from a unique bit storage element; and

(c) the enabling means further comprising:

(1) means for using the bit storage elements to positively assert each corresponding enable bit input of all the memory elements.

[c13] An apparatus of claim 12, its enabling means further comprising:

(a) means for changing the values of one set of bit storage elements while retaining the values of the other set of bit storage elements.

[c14] An apparatus of claim 8, further comprising:

(a) a range decoder, comprising:

(1) a start address input;

(2) an end address input;

(3) a plurality of bit outputs, each of which has a unique address; and

(4) means for concurrently positively asserting all the bit outputs whose addresses are: (A) no less than the value at the start address input, and (B) no more than the value at the end address input, while negatively

asserting all the other bit outputs;

(b) means for connecting each of all the memory elements to a unique bit output of the range decoder, thus each of all the memory elements having a unique element address;

(c) the input/output control unit further comprising:

(1) controlling means for providing the start address input, and the end address input to the range decoder; and

(d) the enabling means further comprising:

(1) means for positively asserting the enable bit inputs of the memory elements whose element addresses are: (A) no less than a start address, and (B) no more than an end address.

[c15] An apparatus of claim 8, further comprising:

(a) a general decoder, comprising:

(1) a start address input;

(2) an end address input;

(3) a carry number input;

(4) a plurality of bit outputs, each of which has a unique address; and

(5) means for concurrently positively asserting all the bit outputs whose addresses are: (A) no less than the value at the start address input, (B) no more than the value at the end address input, and (C) an integer in-

crement of the value at the carry number input starting from the value at the start address input, while negatively asserting all the other bit outputs;

(b) means for connecting each of all the memory elements to a unique bit output of the general decoder, thus each of all the memory elements having a unique element address;

(c) the input/output control unit further comprising:

(1) controlling means for providing the start address input, the end address input, and the carry number input to the general decoder; and

(d) the enabling means further comprising:

(1) means for positively asserting the enable bit inputs of the memory elements whose element addresses are: (A) no less than a start address, (B) no more than an end address, and (C) an integer increment of a carry number starting from the start address.

[c16] An apparatus of claim 15, its general decoder further comprising:

(a) the value of the carry number input being no larger than the square root of the total memory element count of the apparatus.

[c17] An apparatus of claim 15, further comprising:

(a) a priority encoder, comprising:

(1) a plurality of bit inputs, each of which corresponds to a unique address;

(2) a no-hit bit output, which is positively asserted when none of the bit inputs is positively asserted;

(3) a priority high bit input; and

(4) an address output, when the no-hit bit output being negatively asserted, the address output containing either (A) the highest address of the bit inputs which are positively asserted when the priority high bit input is positively asserted, or (B) the lowest address of the bit inputs which are positively asserted when the priority high bit input is negatively asserted;

(b) a parallel counter, comprising:

(1) a plurality of bit inputs;

(2) a count output;

(3) means for concurrently counting the bit inputs which are positively asserted;

(c) dividing means for obtaining: (A) the quotient, and (B) the value of dividend minus reminder, of dividing a dividend by a divider, the dividend being the value of a subtrahend minus an offset, the dividing means further comprising:

(1) means for inputting the offset into the start address input of the general decoder;

(2) means for inputting the subtrahend to the end

address input of the general decoder;

(3) means for inputting the divider to the carry number input of the general decoder;

(4) means for connecting each of all bit outputs of the general decoder to a unique bit input of the parallel counter, except the bit output at address 0 of the general decoder;

(5) means for outputting the quotient from the count output of the parallel counter;

(6) means for connecting each of all bit outputs of the general decoder to the bit input which has same address of the priority encoder, except (A) the bit output at address 0 of the general decoder, and (B) negatively asserting the bit input at address 0 of the priority encoder;

(7) means for positively asserting the priority high bit input of the priority encoder;

(8) when the no-hit bit output of the priority encoder is positively asserted, means for signaling the divider being 0; and

(9) when the no-hit bit output of the priority encoder is negatively asserted, means for outputting the value of dividend minus reminder from the address output of the priority encoder; and

(d) the instruction means further comprising:

(1) means for obtaining (A) the quotient, and (B) the

value of dividend minus reminder, of dividing a dividend by a divider, the dividend being the value of a subtrahend minus an offset.

[c18] An apparatus of claim 17, further comprising:

(a) a plurality of bit storage elements;

(b) means for connecting:

(1) each enable bit input of all the memory elements from a unique bit storage element; and

(2) each of all the bit storage element from a unique bit output of the general decoder;

(c) saving means for saving the value of the bit output of the general decoder to the bit storage element; and

(d) retaining means for retaining the value of the bit storage elements when obtaining (A) the quotient, and (B) the value of dividend minus reminder, of dividing a dividend by a divider, the dividend being the value of a subtrahend minus an offset.

[c19] An apparatus of claim 17, further comprising:

(a) the priority encoder is constantly of high priority.

[c20] An apparatus of claim 8, further comprising:

(a) each of all its memory elements further comprising:

(1) a plurality of registers; and

(b) register identifying means for identifying each register within its memory element by a unique register num-

ber, the register identifying means further comprising:

(1) the set of register numbers is identical for all of the memory elements; and

(2) the registers which have the same register number are functionally equivalent within their memory elements respectively.

[c21] An apparatus of claim 8, each of all its memory elements further comprising:

(a) at least one addressable register.

[c22] An apparatus of claim 8, further comprising:

(a) element address means for assigning a unique address to each of all the memory elements.

[c23] An apparatus of claim 22, further comprising:

(a) each of all its memory elements further comprising:

(1) one addressable register; and

(b) means for using the element address as the register address for each of all the addressable registers.

[c24] An apparatus of claim 22, further comprising:

(a) each of all its memory elements further comprising:

(1) a plurality of addressable registers;

(b) register identifying means for identifying each addressable register within each memory element by a unique register number, the register identifying means

further comprising:

(1) the set of register number is identical for all of the memory elements; and

(2) the registers which have the same register number are functionally equivalent within their memory elements respectively; and

(c) register addressing means for using the combination of the element address and the register number as the register address for each of all the addressable registers.

[c25] An apparatus of claim 24, its register addressing means further comprising:

(a) using the register number as the higher portion of the addressable register address so that functionally equivalent registers within all memory elements form a continuous register address range.

[c26] An apparatus of claim 24, its register addressing means further comprising:

(a) using the register number as the lower portion of the addressable register address so that all addressable registers within each memory elements form a continuous register address range.

[c27] An apparatus of claim 8, each of its memory elements further comprising:

(a) an match bit output;

(b) state means for defining states for the memory element when it is enabled;

(c) matching means for positively asserting the match bit output when the memory element is in a required state; and

(d) the disabling means further comprising means for negatively asserting the match bit output when the enable bit input is negatively asserted.

[c28] An apparatus of claim 27, each of all the memory elements further comprising:

(a) a bit storage element; and

(b) saving means for saving the value of the match bit output in the bit storage element when the memory element is enabled.

[c29] An apparatus of claim 28, each of all the memory elements further comprising:

(a) neighboring means for reading the saved value of the match bit output of the memory element whose element address is either immediately lower or immediately higher than the element address of the memory element itself;

(b) combining means for using the saved value of the match bit output of the selected neighboring memory element in defining the state of the memory element itself; and

(c) transferring means for using the saved value of the match bit output of the selected neighboring memory element as the state of the memory element itself.

[c30] An apparatus of claim 27, further comprising:

(a) a parallel counter, comprising:

(1) a plurality of bit inputs,

(2) a count output,

(3) means for concurrently counting the bit inputs which are positively asserted;

(b) means for connecting:

(1) the match bit output of each of all the memory elements to a unique bit input of the parallel counter, and

(2) the count output of the parallel counter to the input/output control unit;

(c) the concurrent means further comprising:

(1) matching means for specifying the required state for matching concurrently to all the memory elements by the data stored in each enabled memory element and a matching requirement; and

(1) counting means for concurrently counting the enabled memory elements whose match bit outputs are positively asserted; and

(d) the instruction means further comprising:

(1) means for concurrently specifying a matching re-

quirement to each of all the memory elements; and

(2) means for writing the count of the enabled memory elements which satisfy the matching requirement to the external connection of the apparatus.

[c31] Steps for using the apparatus of claim 30, further comprising:

(a) steps for concurrently defining or concurrently changing the selection of the enabled memory elements for matching; and

(b) steps for concurrently specifying a matching requirement to each of all the memory elements; and

(c) steps for concurrently counting the enabled memory elements each of which satisfies the matching requirement.

[c32] An apparatus of claim 27, further comprising:

(a) a priority encoder, comprising:

(1) a plurality of bit inputs, each of which corresponds to a unique address;

(2) a no-hit bit output, which is positively asserted when none of the bit inputs is positively asserted;

(3) a priority high bit input; and

(4) an address output, when the no-hit bit output being negatively asserted, the address output containing either (A) the highest address of the bit inputs which are positively asserted when the priority

high bit input is positively asserted, or (B) the lowest address of the bit inputs which are positively asserted when the priority high bit input is negatively asserted;

(b) means for connecting:

(1) the match bit output of each of all the memory elements to a unique bit input of the priority encoder, thus each of all the memory elements having an address;

(2) the priority high bit input of the priority encoder from the input/output control unit; and

(3) the no-hit bit output and the address output of the priority encoder to the input/output control unit;

(c) the concurrent means further comprising:

(1) matching means for specifying the required state for matching concurrently to all the memory elements by the data stored in each enabled memory element and a matching requirement;

(2) null means for signaling none of the enabled memory elements whose match bit outputs are positively asserted; and

(3) addressing means for finding either the highest or the lowest element address of the enabled memory elements whose match bit outputs are positively asserted; and

(d) the instruction means further comprising:

(1) means for concurrently specifying a matching requirement to each of all the memory elements;

(2) means for writing a predefined value to the external connection of the apparatus if no enabled memory element satisfying the matching requirement; and

(3) means for writing to the external connection of the apparatus either (A) the highest or (B) the lowest address among those of the enabled memory elements which satisfy the matching requirement.

[c33] Steps for using the apparatus of claim 32, further comprising:

(a) steps for concurrently defining or concurrently changing the selection of the enabled memory elements for matching;

(b) steps for concurrently specifying a matching requirement to each of all the memory elements;

(c) steps for concurrently finding none of the enabled memory elements satisfying the matching requirement;

(d) steps for concurrently finding the highest address of the enabled memory element which satisfies the matching requirement;

(e) steps for concurrently finding the lowest address of the enabled memory element which satisfies the matching requirement; and

(f) steps for concurrently enumerating the addresses of the enabled memory elements each of which satisfies the matching requirement.

[c34] An apparatus of claim 32, further comprising:

(a) a parallel counter, comprising:

(1) a plurality of bit inputs,

(2) a count output,

(3) means for concurrently counting the bit inputs which are positively asserted;

(b) means for connecting:

(1) the match bit output of each of all the memory elements to a unique bit input of the parallel counter, and

(2) the count output of the parallel counter to the input/output control unit;

(c) the concurrent means further comprising:

(1) matching means for specifying the required state for matching concurrently to all the memory elements by the data stored in each enabled memory element and a matching requirement; and

(2) counting means for concurrently counting the enabled memory elements whose match bit outputs are positively asserted; and

(d) the instruction means further comprising:

(1) means for concurrently specifying a matching re-

quirement to each of all the memory elements; and

(2) means for writing to the external connection of the apparatus the count of the enabled memory elements which satisfy the matching requirement.

[c35] Steps for using the apparatus of claim 34, further comprising:

(a) steps for concurrently defining or concurrently changing the selection of the enabled memory elements for matching;

(b) steps for concurrently specifying a matching requirement to each of all the memory elements;

(c) steps for concurrently finding none of the enabled memory elements satisfying the matching requirement;

(d) steps for concurrently finding the highest address of the enabled memory element which satisfies the matching requirement;

(e) steps for concurrently finding the lowest address of the enabled memory element which satisfies the matching requirement;

(f) steps for concurrently enumerating the addresses of the enabled memory elements each of which satisfies the matching requirement; and

(g) steps for concurrently counting the enabled memory elements each of which satisfies the matching requirement.

[c36] An apparatus of claim 34, each of all its memory elements further comprising:

(a) a general decoder, comprising:

(1) a start address input;

(2) an end address input;

(3) a carry number input;

(4) a plurality of bit outputs, each of which has a unique address; and

(5) means for concurrently positively asserting all the bit outputs whose addresses are: (A) no less than the value at the start address input, (B) no more than the value at the end address input, and (C) an integer increment of the value at the carry number input starting from the value at the start address input, while negatively asserting all the other bit outputs;

(b) means for connecting each of all the memory elements to the bit output of the general decoder which has the same address as the memory element;

(c) the input/output control unit further comprising:

(1) controlling means for providing the start address input, the end address input, and the carry number input to the general decoder; and

(d) the enabling means further comprising:

(1) means for positively asserting the enable bit inputs of the memory elements whose element ad-

dresses are: (A) no less than a start address, (B) no more than an end address, and (C) an integer increment of a carry number starting from the start address.

[c37] An apparatus of claim 36, further comprising:

(a) dividing means for obtaining (A) the quotient and (B) the value of dividend minus reminder, of dividing a dividend by a divider, the dividend being the value of a subtrahend minus an offset, the dividing means further comprising:

(1) means for inputting the offset into the start address input of the general decoder;

(2) means for inputting the subtrahend to the end address input of the general decoder;

(3) means for inputting the divider to the carry number input of the general decoder;

(4) means for connecting each of all bit outputs of the general decoder to a unique bit input of the parallel counter, except the bit output at address 0 of the general decoder;

(5) means for outputting the quotient from the count output of the parallel counter;

(6) means for connecting each of all bit outputs of the general decoder to the bit input which has same address of the priority encoder, except (A) the bit

output at address 0 of the general decoder, and (B) negatively asserting the bit input at address 0 of the priority encoder;

(7) means for positively asserting the priority high bit input of the priority encoder;

(8) when the no-hit bit output of the priority encoder is positively asserted, means for signaling the divider being 0; and

(9) when the no-hit bit output of the priority encoder is negatively asserted, means for outputting the value of dividend minus reminder from the address output of the priority encoder; and

(b) the instruction means further comprising:

(1) means for obtaining (A) the quotient, and (B) the value of dividend minus reminder, of dividing a dividend by a divider, the dividend being the value of a subtrahend minus an offset.

[c38] An apparatus of claim 37, further comprising:

(a) a plurality of bit storage elements;

(b) means for connecting:

(1) each enable bit input of all the memory elements from a unique bit storage element; and

(2) each of all the bit storage element from a unique bit output of the general decoder;

(c) saving means for saving the value of each of all the

bit outputs of the general decoder to the corresponding bit storage element; and

(d) retaining means for retaining the value of the bit storage elements when obtaining (A) the quotient, and (B) the value of dividend minus reminder, of dividing a dividend by a divider, the dividend being the value of a subtrahend minus an offset.

[c39] An apparatus of claim 27, each of its memory elements further comprising:

(a) at least one status bit;

(b) status means for either (A) positively or (B) negatively asserting any of the status bits, and

(c) the state means further comprising means for using the values of the status bit(s) to define the state of the memory element.

[c40] An apparatus of claim 27, each of its memory elements further comprising:

(a) the required state being a predefined state.

[c41] An apparatus of claim 27, further comprising:

(a) the concurrent bus further carrying a condition specification to each of all the memory elements; and

(b) the matching means further comprising:

(1) specifying means for using the condition specification of the concurrent bus to specify the required

state, and

(2) determining means for determining if the state of the memory element matches the required state which has been specified by the condition specification of the concurrent bus.

[c42] An apparatus of claim 27, each of its memory elements further comprising:

(a) an unequal comparator, comprising:

(1) a first input;

(2) a second input; and

(3) a bit output, which is positively asserted when any bit of the first input is asserted differently from the corresponding bit of the second input;

(b) the state means further comprising means for using the bit output of the unequal comparator to define the state of the memory element.

[c43] An apparatus of claim 42, the unequal comparator in each of its memory elements further comprising:

(a) a bus XOR gate, comprising:

(1) a first input;

(2) a second input; and

(3) a output, each of its bit being positively asserted when the corresponding bit of the first input is asserted differently from the corresponding bit of the second input;

(b) a OR gate, comprising:

(1) a plurality of bit inputs; and

(2) a bit output, which is positively asserted when any of its bit inputs is positively asserted;

(c) means for connecting:

(1) the first input of the comparator to the first input of the bus XOR gate;

(2) the second input of the comparator to the second input of the bus XOR gate;

(3) each bit of the output of the bus XOR gate to an unique bit input of the OR gate; and

(4) the bit output of the OR gate to the bit output of the comparator.

[c44] An apparatus of claim 42, each of its memory elements further comprising:

(a) means for connecting one register to the first input of the unequal comparator, the register being called the comparable register of the memory element.

[c45] An apparatus of claim 44, each of its memory elements further comprising:

(a) the comparable register being addressable.

[c46] An apparatus of claim 44, each of its memory elements further comprising:

(a) means for connecting one addressable register other

than the comparable register to the second input of the unequal comparator.

[c47] An apparatus of claim 42, further comprising:

(a) the concurrent bus further carrying a condition datum to all the memory elements; and

(b) each of all the memory elements further comprising:

(1) means for connecting the condition datum of the concurrent bus to the second input of the unequal comparator.

[c48] An apparatus of claim 42, further comprising:

(a) the concurrent bus further carrying a mask to each of all the memory elements;

(b) each of all the memory elements further comprising:

(1) a bus AND gate, comprising:

(A) a first input;

(B) a second input;

(C) a output, each of its bit being positively asserted when the corresponding bits of the first input and the second input are both positively asserted; and

(2) means for connecting:

(A) the mask of the concurrent bus to the second input of the bus AND gate; and

(B) the output of the bus AND gate to the first input

of the unequal comparator; and

(c) the concurrent means further comprising:

(1) masking means for masking the first input of the AND gate with the mask of the concurrent bus before comparing it with the second input of the unequal comparator.

[c49] An apparatus of claim 42, further comprising:

(a) the concurrent bus further carrying a condition code bit to all the memory elements; and

(b) each of all the memory elements further comprising:

(1) a XOR gate, comprising:

(A) a first bit input;

(B) a second bit input; and

(C) a bit output, which is positively asserted when the first bit input is asserted differently from the second bit input;

(2) means for connecting:

(A) the bit output of the unequal comparator to the first bit input of the XOR gate; and

(B) the condition code bit of the concurrent bus to the second bit input of the XOR gate;

(c) the concurrent means further comprising:

(1) specifying means for using the condition code bit of the concurrent bus to specify the required state to

be either (A) equal, or (B) unequal;

(2) determining means for determining if the state which comprises the output value of the unequal comparator of each of all the enabled memory elements matches the required state which has been specified by the condition code bit of the concurrent bus.

[c50] An apparatus of claim 49, each of its memory elements further comprising:

(a) an AND gate, comprising:

(1) a first bit input and a second bit input; and

(2) a bit output, which is positively asserted when both bit inputs are positively asserted;

(b) means for connecting:

(1) the enable bit input of the memory element to the first bit input of the AND gate;

(2) the bit output of the XOR gate to the second bit input of the AND gate; and

(3) the bit output of the AND gate to the match bit output of the memory element.

[c51] An apparatus of claim 49, further comprising:

(a) the concurrent bus further carrying a condition datum to all the memory elements;

(b) each of all the memory elements further comprising means for connecting:

(1) a register to the first input of the comparator, the register being called the comparable register of the memory element; and

(2) the condition datum to the second input of the comparator of each of all the memory elements.

(c) the concurrent means further comprising:

(1) means for positively asserting the match bit outputs of each of all the enabled memory elements whose comparable register having value satisfying the comparing requirement of either (A) equal, or (B) unequal, with the value of the condition datum of the concurrent bus.

[c52] An apparatus of claim 49, further comprising:

(a) the concurrent bus further carrying to all the memory elements:

(1) a condition datum;

(2) a mask;

(b) each of its memory elements further comprising:

(1) a bus AND gate, comprising:

(A) a first input;

(B) a second input; and

(C) a output, each of its bit being positively asserted when the corresponding bits of the first input and the second input are both positively as-

serted; and

(2) means for connecting:

(A) a register to the first input of the bus AND gate, the register being called the comparable register of the memory element; and

(A) the mask of the concurrent bus to the second input of the bus AND gate;

(C) the condition datum of the concurrent bus to the second input of the unequal comparator; and

(c) the concurrent means further comprising:

(1) means for positively asserting the match bit outputs of each of all the enabled memory elements whose comparable registers after being masked by the mask of the concurrent bus having value satisfying the comparing requirement of either (A) equal, or (B) unequal, with the value of the condition datum of the concurrent bus.

[c53] Searching steps for searching from data stored in the comparable registers of the memory elements in an apparatus of claim 51, for a value to be searched, according to a searching requirement, the searching steps further comprising:

(a) steps for concurrently defining or concurrently changing the selection of the memory elements for

searching;

(b) steps for concurrently specifying the value to be searched by the concurrent bus; and

(c) steps for concurrently specifying by the concurrent bus the searching requirement to be either (A) equal or (B) unequal between the value to be searched and the value of the comparable register of each of all the enabled memory element.

[c54] An apparatus of claim 54, further comprising:

(a) a range decoder, comprising:

(1) a start address input;

(2) an end address input;

(3) a plurality of bit outputs, each of which has a unique address; and

(4) means for concurrently positively asserting all the bit outputs whose addresses are: (A) no less than the value at the start address input, and (B) no more than the value at the end address input, while negatively asserting all the other bit outputs;

(b) means for connecting each of all the memory elements to a unique bit output of the range decoder, thus each of all the memory elements having a unique address;

(c) the input/output control unit further comprising:

(1) controlling means for providing the start address

input, and the end address input to the range decoder;

(d) the enabling means further comprising:

(1) means for positively asserting the enable bit inputs of the memory elements whose element addresses are: (A) no less than a start address, and (B) no more than an end address;

(e) the concurrent bus further carrying a self code bit to all the memory elements;

(f) each of all the memory elements further comprising:

(1) a neighboring bit input;

(2) an one-bit neighboring register; and

(3) saving means for saving the match state of the memory element to be either (A) match, or (B) not match, to the neighboring register when the memory element is enabled;

(g) neighboring means for connecting:

(1) the neighboring register of each of all the memory elements to the neighboring bit input of the memory element whose element address is immediately lower than the element address of the memory element itself;

(h) the concurrent means further comprising:

(1) when the self code bit of the concurrent bus is positively asserted, self means for positively asserting the match bit output of each of all the enabled

memory element when the bit output of the XOR gate is positively asserted; and

(2) when the self code bit of the concurrent bus is negatively asserted, combining means for positively asserting the match bit output of each of all the enabled memory element when (A) the bit output of the the XOR gate of the memory element itself is positively asserted, and (B) the neighboring register of the memory element whose element address is immediately higher than the memory element itself is positively asserted.

[c55] Searching steps for searching from data stored in the comparable registers of an apparatus of claim 54, for a value to be searched which has several portions, with each portion spanning a memory element, the searching steps further comprising:

(a) steps for concurrently defining or concurrently changing the selection of the enabled memory elements for searching;

(b) steps for storing each of all array item by multiple neighboring memory elements in the same order;

(c) steps for positively asserting the neighboring register of each of all the memory elements when the comparable register equals the first portion of the value to be matched;

(d) in the order from the first portion to the last portion of the value to be searched, steps for positively asserting the neighboring register of each of all the memory elements when: (A) the comparable register equals the corresponding portion of the value to be matched; and (B) the neighboring memory element of immediately lower order has positively asserted neighboring register; and

(e) steps for using the match bit output to signal the memory element which contains the last portion of each of all the neighboring memory elements which together hold a datum that matches the value to be searched.

[c56] An apparatus of claim 27, each of its memory elements further comprising:

(a) a value comparator, comprising:

(1) a first input;

(2) a second input;

(3) an equal bit output, which is positively asserted when the value of the first input equals the value of the second input; and

(4) a larger bit output, which is either (A) positively asserted when the value at the first input is larger than the value at the second input, or (B) negatively asserted when the value at the first input is smaller than the value at the second input;

(b) the state means further comprising means for using

(A) the equal bit output of the value comparator and (B) the larger bit output of the value comparator to define the state of the memory element.

[c57] An apparatus of claim 56, each of its memory elements further comprising:

(a) the value comparator being a parallel comparator, comprising:

(1) a first input;

(2) a second input;

(3) an equal bit output;

(4) a larger bit output; and

(5) means for concurrently comparing the value at the first input and the value at the second input so that: (A) the equal bit output is positively asserted when the value at the first is equal to the value at the second input; (B) the larger bit output is positively asserted when the value at the first is larger than the value at the second input; and (C) the larger bit output is negatively asserted when the value at the first is smaller than the value at the second input.

[c58] An apparatus of claim 56, each of its memory elements further comprising:

(a) means for connecting one register to the first input of the value comparator, the register being called the comparable register of the memory element.

[c59] An apparatus of claim 56, each of its memory elements further comprising:

(a) the comparable register being addressable.

[c60] An apparatus of claim 58, each of its memory elements further comprising:

(a) means for connecting one addressable register other than the comparable register to the second input of the value comparator.

[c61] An apparatus of claim 56, further comprising:

(a) the concurrent bus further carrying a condition datum to all the memory elements; and

(b) each of all the memory elements further comprising:

(1) means for connecting the condition datum of the concurrent bus to the second input of the value comparator.

[c62] An apparatus of claim 56, further comprising:

(a) the concurrent bus further carrying a mask to each of all the memory elements;

(b) each of all the memory elements further comprising:

(1) a bus AND gate, comprising:

(A) a first input;

(B) a second input;

(C) a output, each of its bit being positively as-

serted when the corresponding bits of the first input and the second input are both positively asserted; and

(2) means for connecting:

(A) the mask of the concurrent bus to the second input of the bus AND gate; and

(B) the output of the bus AND gate to the first input of the value comparator; and

(c) the concurrent means further comprising:

(1) masking means for masking the first input of the bus AND gate before comparing it with the second input of the value comparator.

[c63] An apparatus of claim 56, further comprising:

(a) the concurrent bus further carrying a condition code to all the memory elements, comprising:

(1) a else code bit;

(2) an equal code bit; and

(3) a larger code bit;

(b) each of all the memory elements further comprising:

(1) a matching logic table, further comprising:

(A) the condition code input, which inputs the condition code of the concurrent bus;

(B) a case input, which inputs the bit outputs of the value comparator, comprising an equal case bit in-

put; and a larger case bit input;

(C) a match bit output; and

(D) means for asserting the match bit output according to the following function table:

	Condition	000	001	01X	11X	100	101
Case	Meaning	<	>	!=	==	<=	>=
00	<	1	0	1	0	1	0
01	>	0	1	1	0	0	1
1X	==	0	0	0	1	1	1

(c) the concurrent means further comprising:

(1) specifying means for using the condition code of the concurrent bus to specify the required state of the memory element as one of: (A) equal, (B) unequal, (C) larger, (D) smaller, (E) larger and equal, and (F) smaller and equal; and

(2) determining means for determining if the state which comprises the output value of the value comparator of each of all the enabled memory element matches the required state which has been specified by the condition code of the concurrent bus.

[c64] An apparatus of claim 63, each of its memory elements further comprising:

(a) the matching logic table comprising a standard two-layer logic.

[c65] An apparatus of claim 63, each of its memory elements further comprising:

(a) a AND gate, comprising:

(1) a first bit input and a second bit input; and

(2) a bit input, which is positively asserted when both bit inputs are positively asserted; and

(b) means for connecting:

(1) the matching bit output of the matching logic table to the first bit input of the AND gate;

(2) the enable bit input of the memory element to the second bit input of the AND gate; and

(3) the bit output of the AND gate to the match bit output of the memory element.

[c66] An apparatus of claim 63, further comprising:

(a) the concurrent bus further carrying a condition datum to all the memory elements;

(b) each of its memory elements further comprising means for connecting:

(1) a register to the first input of the value comparator, the register being called the comparable register of the memory element; and

(2) the condition datum of the concurrent bus to the second input of the value comparator; and

(c) the concurrent means further comprising:

(1) means for positively asserting the match bit outputs of each of all the enabled memory elements whose comparable registers having value satisfying the comparing requirement of either (A) equal, or (B)

unequal, or (C) larger than, or (D) smaller than, or (E) equal or larger than, or (F) equal or smaller than, with the value of the condition datum of the concurrent bus.

[c67] An apparatus of claim63, further comprising:

(a) the concurrent bus further carrying to each of all the memory elements:

(1) a condition datum; and

(2) a mask;

(b) each of its memory elements further comprising:

(1) a bus AND gate, comprising:

(A) a first input;

(B) a second input; and

(C) a output, each of its bit being positively asserted when the corresponding bits of the first input and the second input are both positively asserted; and

(2) means for connecting:

(A) a register to the first input of the bus AND gate, the register being called the comparable register of the memory element;

(B) the mask of the concurrent bus to the second input of the bus AND gate;

(C) the output of the bus AND gate to the first input

of the value comparator; and

(D) the condition datum of the concurrent bus to the second input of the value comparator; and

(c) the concurrent means further comprising:

(1) means for positively asserting the match bit outputs of each of all the enabled memory elements whose comparable registers after being masked by the mask of the concurrent bus having value satisfying the comparing requirement of either (A) equal, or (B) unequal, or (C) larger than, or (D) smaller than, or (E) equal or larger than, or (F) equal or smaller than, with the value of the condition datum of the concurrent bus.

[c68] Comparing steps for comparing the data stored in the comparable registers of the memory elements in an apparatus of claim 66, for a value to be searched, according to a comparison requirement, the searching steps further comprising:

(a) steps for concurrently defining or concurrently changing the selection of the memory elements for comparing;

(b) steps for concurrently specifying the value to be compared by the concurrent bus; and

(c) steps for concurrently specifying by the concurrent bus the comparison requirement to be either (A) equal,

or (B) unequal, or (C) smaller, or (D) larger, or (E) equal or smaller, or (F) equal or larger, between the value to be compared and the value of the comparable register of each of all the enabled memory element.

[c69] An apparatus of claim 66, further comprising:

(a) a general decoder, comprising:

(1) a start address input;

(2) an end address input;

(3) a carry number input;

(4) a plurality of bit outputs, each of which has a unique address; and

(5) means for concurrently positively asserting all the bit outputs whose addresses are: (A) no less than the value at the start address input, (B) no more than the value at the end address input, and (C) an integer increment of the value at the carry number input starting from the value at the start address input, while negatively asserting all the other bit outputs;

(b) means for connecting each of all the memory elements to a unique bit output of the general decoder, thus each of all the memory elements having a unique element address;

(c) the input/output control unit further comprising:

(1) controlling means for providing the start address input, the end address input, and the carry number

input to the general decoder;

(d) the enabling means further comprising:

(1) means for positively asserting the enable bit inputs of the memory elements whose element addresses are: (A) no less than the start address, (B) no more than the end address, and (C) an integer increment of the carry number starting from the start address;

(e) the concurrent bus further carrying an operation code to each of all the memory elements, the operation code comprising:

(1) a select code bit;

(2) a self code bit; and

(3) a transfer code bit;

(f) each of all the memory elements further comprising:

(1) an one-bit neighboring register;

(2) saving means for saving the match state of the memory element to be either (A) match, or (B) not match, to the neighboring register when the memory element is enabled;

(3) a register multiplexer, comprising:

(A) a first bit input;

(B) a second bit input;

(C) a bit output; and

(D) a selection bit input, which connect the first bit

input to the bit output when positively asserted, or the second bit input to the bit output when negatively asserted;

(g) neighboring means for connecting:

(1) the neighboring register of each of all the memory elements to the first bit input of the register multiplexer of the memory element whose element address is immediately higher than the element address of the memory element itself; and

(2) the neighboring register of each of all the memory elements to the second bit input of the register multiplexer of the memory element whose element address is immediately lower than the element address of the memory element itself;

(h) the concurrent means further comprising:

(1) when (A) the self code bit of the concurrent bus is negatively asserted, (B) the transfer code bit of the concurrent bus is negatively asserted, and (C) the select code bit of the concurrent bus is negatively asserted, lower combining means for positively asserting the the neighboring register of the memory element itself when (A) the match bit output of the match logic table of the memory element itself is positively asserted, and (B) the neighboring register of the memory element whose element address is

immediately lower is positively asserted;

(2) when (A) the self code bit of the concurrent bus is negatively asserted, (B) the transfer code bit of the concurrent bus is negatively asserted, and (C) the select code bit of the concurrent bus is positively asserted, higher combining means for positively asserting the neighboring register of the memory element itself when (A) the match bit output of the match logic table of the memory element itself is positively asserted, and (B) the neighboring register of the memory element whose element address is immediately higher is positively asserted;

(3) when (A) the self code bit of the concurrent bus is negatively asserted, (B) the transfer code bit of the concurrent bus is positively asserted, (C) the select code bit of the concurrent bus is negatively asserted, and (D) the neighboring register is positively asserted, lower transferring means for copy the neighboring register of the memory element itself from the neighboring register of the memory element whose element address is immediately lower;

(4) when (A) the self code bit of the concurrent bus is negatively asserted, (B) the transfer code bit of the concurrent bus is positively asserted, (C) the select code bit of the concurrent bus is positively asserted, and (D) the neighboring register is positively as-

serted, higher transferring means for copy the neighboring register of the memory element itself from the neighboring register of the memory element whose element address is immediately higher; and
(5) in any other case, self means for asserting the neighboring register of the memory element itself with the value of the match bit output of the match logic table.

[c70] Combined comparing steps for comparing array items stored in the comparable registers of an apparatus as claim 69 with a value to be compared which has several portions, each array item having corresponding multiple portions, with each portion spanning a memory element, the comparing steps further comprising:
(a) steps for concurrently defining or concurrently changing the selection of the enabled memory elements for searching;
(b) steps for storing each array item by multiple neighboring memory elements in the order of significance;
(c) steps for positively asserting the neighboring register of each of all the memory elements whose comparable register holds the most significant portion that equals the most significant portion of the value to be compared;
(d) in the decreased significance from the most significant memory element to the least significant memory el-

ement of each of all array items, steps for positively asserting the neighboring register of each of all the memory elements when: (A) the comparable register equals the corresponding portion of the value to be compared; and (B) the neighboring memory element of immediately higher significance has positively asserted neighboring register;

(e) in the increased significance from the least significant memory element to the most significant memory element of each of all array items:

(1) steps for positively asserting the neighboring register of each of all the memory elements when the value of the comparable register satisfies the condition code of the concurrent bus with the corresponding portion of the value to be compared when the neighboring register of the memory element itself is originally negatively asserted; and

(2) steps for transferring the neighboring register of each of all the memory elements from the neighboring register of the neighboring memory element of immediately lower significance when the neighboring register of the memory element itself is originally positively asserted; and

(f) steps for using the match bit output of the most significant memory element of each of all array items to signal the matching of the array items.

[c71] An apparatus of claim 56, further comprising:

(a) a parallel counter, comprising:

(1) a plurality of bit inputs,

(2) a count output,

(3) means for concurrently counting the bit inputs which are positively asserted;

(b) means for connecting:

(1) the match bit output of each of all the memory elements to a unique bit input of the parallel counter, and

(2) the count output of the parallel counter to the input/output control unit;

(c) the concurrent means further comprising:

(1) comparing means for defining the required state for matching concurrently to all the memory element by the data stored in each enabled memory element and a comparison requirement; and

(2) counting means for concurrently counting the enabled memory element whose match bit outputs are positively asserted; and

(d) the instruction means further comprising:

(1) means for concurrently specifying a comparison requirement to each of all the memory elements; and

(2) means for writing the count of the enabled memory elements each of which satisfies the comparison

requirement.

[c72] Steps for using the apparatus of claim 70,1further comprising:

(a) steps for concurrently defining or concurrently changing the selection pattern of the enabled memory elements for matching;

(b) steps for concurrently specifying a comparison requirement to each of all the memory elements;

(c) steps for storing an array by the apparatus;

(d) steps for concurrently counting the array items each of which satisfies the comparison requirement; and

(e) steps for concurrently constructing a histogram of the array.

[c73] An apparatus of claim 56, further comprising:

(a) a priority encoder, comprising:

(1) a plurality of bit inputs, each of which corresponds to a unique address;

(2) a no-hit bit output, which is positively asserted when none of the bit inputs is positively asserted;

(3) a priority high bit input; and

(4) an address output, when the no-hit bit output being negatively asserted, the address output containing either (A) the highest address of the bit inputs which are positively asserted when the priority high bit input is positively asserted, or (B) the lowest

address of the bit inputs which are positively asserted when the priority high bit input is negatively asserted;

(b) means for connecting:

(1) the match bit output of each of all the memory elements to a unique bit input of the priority encoder, thus each of all the memory elements having an address;

(2) the priority high bit input of the priority encoder from the input/output control unit; and

(3) the no-hit bit output and the address output of the priority encoder to the input/output control unit;

(c) the concurrent means further comprising:

(1) comparing means for specifying the required state for matching concurrently to all the memory element by the data stored in each enabled memory element and a comparison requirement;

(2) null means for signaling none of the enabled memory elements whose match bit output is positively asserted; and

(3) addressing means for finding either the highest or the lowest element address of the enabled memory element whose match bit output is positively asserted; and

(d) the instruction means further comprising:

(1) means for concurrently specifying a comparison

requirement to each of all the memory elements;

(2) means for writing a predefined value to the external connections of the apparatus if no enabled memory element satisfying the comparison requirement; and

(3) means for writing to the external connections of the apparatus either (A) the highest or (B) the lowest address of the enabled memory element which satisfies the comparison requirement.

[c74] Steps for using the apparatus of claim 73, further comprising:

(a) steps for concurrently defining or concurrently changing the selection of the enabled memory elements for comparing;

(b) steps for concurrently specifying a comparison requirement to each of all the memory elements;

(c) steps for storing an array by the apparatus;

(d) steps for concurrently finding none of the array item which satisfies the comparison requirement;

(e) steps for concurrently finding the highest address of the array item which satisfies the comparison requirement;

(f) steps for concurrently finding the lowest address of the array item which satisfies the comparison requirement;

(g) steps for concurrently enumerating addresses of the array items each of which satisfies the comparison requirement;

(h) steps for concurrently finding a global boundary of the array; and

(i) steps for concurrently finding a global limit of the array.

[c75] An apparatus of claim 73, further comprising:

(a) a parallel counter, comprising:

(1) a plurality of bit inputs,

(2) a count output,

(3) means for concurrently counting the bit inputs which are positively asserted;

(b) means for connecting:

(1) the match bit output of each of all the memory elements to a unique bit input of the parallel counter, and

(2) the count output of the parallel counter to the input/output control unit;

(c) the concurrent means further comprising:

(1) comparing means for specifying the required state for matching concurrently to all the memory element by the data stored in each enabled memory element and a comparison requirement; and

(2) counting means for concurrently counting the en-

abled memory element whose match bit outputs are positively asserted; and

(d) the instruction means further comprising:

(1) means for concurrently specifying a comparison requirement to each of all the memory elements; and

(2) means for writing the count of the enabled memory elements each of which satisfies the comparison requirement.

[c76] Steps for using the apparatus of claim 75, further comprising:

(a) steps for concurrently defining or concurrently changing the selection of the enabled memory elements for matching;

(b) steps for concurrently specifying a comparison requirement to each of all the memory elements;

(c) steps for storing an array by the apparatus;

(d) steps for concurrently finding none of the array item which satisfies the comparison requirement;

(e) steps for concurrently finding the highest address of the array item which satisfies the comparison requirement;

(f) steps for concurrently finding the lowest address of the array item which satisfies the comparison requirement;

(g) steps for concurrently enumerating addresses of the

array items each of which satisfies the comparison requirement;

(h) steps for concurrently finding a global boundaries of the array;

(i) steps for concurrently finding a global limit of the array;

(j) steps for concurrently counting the array items each of which satisfies the comparison requirement; and

(k) steps for concurrently constructing a histogram of the array.

[c77] An apparatus of claim 76, each of all its memory elements further comprising:

(a) a general decoder, comprising:

(1) a start address input;

(2) an end address input;

(3) a carry number input;

(4) a plurality of bit outputs, each of which has a unique address; and

(5) means for concurrently positively asserting all the bit outputs whose addresses are: (A) no less than the value at the start address input, (B) no more than the value at the end address input, and (C) an integer increment of the value at the carry number input starting from the value at the start address input, while negatively asserting all the other bit outputs;

(b) means for connecting each of all the memory elements to the bit output of the general decoder which has the same address as the memory element;

(c) the input/output control unit further comprising:

(1) controlling means for providing the start address input, the end address input, and the carry number input to the general decoder; and

(d) the enabling means further comprising:

(1) means for positively asserting the enable bit inputs of the memory elements whose element addresses are: (A) no less than a start address, (B) no more than an end address, and (C) an integer increment of a carry number starting from the start address.

[c78] An apparatus of claim77, further comprising:

(a) dividing means for obtaining (A) the quotient, and (B) the value of dividend minus reminder, of dividing a dividend by a divider, the dividend being the value of a subtrahend minus an offset, the dividing means further comprising:

(1) means for inputting the offset into the start address input of the general decoder;

(2) means for inputting the subtrahend to the end address input of the general decoder;

(3) means for inputting the divider to the carry num-

ber input of the general decoder;

(4) means for connecting each of all bit outputs of the general decoder to a unique bit input of the parallel counter, except the bit output at address 0 of the general decoder;

(5) means for outputting the quotient from the count output of the parallel counter;

(6) means for connecting each of all bit outputs of the general decoder to the bit input which has same address of the priority encoder, except (A) the bit output at address 0 of the general decoder, and (B) negatively asserting the bit input at address 0 of the priority encoder;

(7) means for positively asserting the priority high bit input of the priority encoder;

(8) when the no-hit bit output of the priority encoder is positively asserted, means for signaling the divider being 0; and

(9) when the no-hit bit output of the priority encoder is negatively asserted, means for outputting the value of dividend minus reminder from the address output of the priority encoder; and

(b) the instruction means further comprising:

(1) means for obtaining (A) the quotient, and (B) the value of dividend minus reminder, of dividing a dividend by a divider, the dividend being the value of a

subtrahend minus an offset.

[c79] An apparatus of claim 78, further comprising:

(a) a plurality of bit storage elements;

(b) means for connecting:

(1) each enable bit input of all the memory elements from a unique bit storage element; and

(2) each of all the bit storage element from a unique bit output of the general decoder;

(c) saving means for saving the value of each of all the bit outputs of the general decoder to the corresponding bit storage element; and

(d) retaining means for retaining the value of the bit storage elements when obtaining (A) the quotient, and (B) the value of dividend minus reminder, of dividing a dividend by a divider, the dividend being the value of a subtrahend minus an offset.

[c80] An apparatus of claim 8, further comprising:

(a) the concurrent bus carrying concurrently to each of all the memory elements:

(1) a read selection code; and

(2) an operation code;

(b) each of all the memory elements further comprising:

(1) a neighboring register, being a register;

(2) a operation register, being a register; and

(3) a register multiplexer, being a bus multiplexer,

comprising:

(A) a plurality of inputs;

(B) an output; and

(C) a selection input, which selects one of the inputs to be connected to the output; and

(4) means for connecting:

(A) the neighboring register to a unique input of the register multiplexer;

(B) the operation register to the output of the register multiplexer; and

(C) the read selection code of the concurrent bus to the selection input of the register multiplexer;

(c) neighboring means for connecting each of all the memory elements to other memory elements, the neighboring means further comprising:

(1) up connecting means for connecting from the neighboring register of each of all the memory elements to a unique input of the register multiplexer of the memory element which has immediately higher element address; and

(2) down connecting means for connecting from the neighboring register of each of all the memory elements to a unique input of the register multiplexer of the memory element which has immediately lower element address;

(d) the concurrent means further comprising:

(1) instructing means for sending an instruction to each of all the memory elements using the concurrent bus;

(2) read selecting means for selecting the same one of the inputs to the output of the register multiplexer of each of all the enabled memory elements;

(3) read means for copying the content of the output of the register multiplexer to the operation register of each of all the enabled memory elements; and

(4) write means for copying the content of the operation register to the neighboring register of each of all the enabled memory elements.

[c81] An apparatus of claim 80, further comprising:

(a) a range decoder, comprising:

(1) a start address input;

(2) an end address input;

(3) a plurality of bit outputs, each of which has a unique address; and

(4) means for concurrently positively asserting all the bit outputs whose addresses are: (A) no less than the value at the start address input, and (B) no more than the value at the end address input, while negatively asserting all the other bit outputs;

(b) means for connecting each of all the memory ele-

ments to a unique bit output of the range decoder, thus each of all the memory elements having a unique address;

(c) the input/output control unit further comprising:

(1) controlling means for providing the start address input, and the end address input to the range decoder;

(d) the enabling means further comprising:

(1) means for positively asserting the enable bit inputs of the memory elements whose element addresses are: (A) no less than a start address, and (B) no more than an end address;

(e) each of all the memory elements further comprising:

(1) the neighboring register being addressable;

(2) the register multiplexer having two inputs; and

(3) only two registers within each memory element;

(f) the concurrent means further comprising:

(1) moving means for concurrently moving the content of all the addressable registers within a register address range either up or down by one addressable register.

[c82] An apparatus of claim 81, each of its memory elements further comprising:

(a) the operation register being made of dynamic memory cells whose storage duration is long enough for car-

rying out the moving means.

[c83] An apparatus of claim 81, its moving means further comprising:
(a) means for concurrently moving the content of all the addressable registers within a register address range to another register address range of the same size.

[c84] Content moving means for moving within the apparatus of claim 81, a data object which occupies a continuous register address range, the content moving means comprising:
(a) moving means for moving a data object within the apparatus to another register address range without overwriting any other useful stored data;
(b) inserting means for inserting a data object into the apparatus without overwriting any other useful stored data;
(c) enlarging means for enlarging a data object within the apparatus without overwriting any other useful stored data;
(d) shrinking means for shrinking a data object within the apparatus without leaving unused addressable registers at where the data object originally resides;
(e) removing means for removing a data object from the apparatus without leaving unused addressable registers at where the data object originally resides; and

(f) packing means for keeping the used portion of the addressable registers adjacent to each other so that the data within the apparatus are closely packed during inserting, enlarging, shrinking, removing, and moving data object within the apparatus.

[c85] Address independent means for identifying the stored data objects within an apparatus which has content moving means as claimed in claim 84, each by a unique number independent of the addresses which are associated with the storing of the data object in the apparatus, the address independent means comprising:
(a) means for identifying each data objects in the apparatus by an object ID which is a unique number, independent of the addresses which are associated with the storing of the data object in the apparatus;
(b) means for adding a new data object of a specified size and obtaining the corresponding new object ID;
(c) means for removing a such identified data object;
(d) means for changing the size of a such identified object by specifying a new size of the data object;
(e) means for exclusively accessing any part of a such identified data object by an offset into the data object;
(f) means for refusing access when a such access is beyond the storage range of the such identified data object; and

(g) means for containing a child data object within a parent data object, and (A) adjusting the size of the parent data object accordingly when operating any of its child data objects; and (B) adjusting the size and location of the child data object when operating any of its parent object.

[c86] Program using steps for using an apparatus which has content moving means as claimed in claim 84 to hold the data objects of a program, the program using steps comprising:
(a) steps for using a unified data memory instead of a stack memory and a heap memory; and
(b) steps for changing the range and precision of a numerical data object dynamically.

[c87] An apparatus of claim 80, it connecting means further comprising:
(a) means for connecting from the neighboring register of each of all the memory elements whose element address is $(M\hat{}j\ k + \Sigma_{l=0\ldots(j-1)}(M\hat{}l))$ to a unique input of the register multiplexer of the memory element whose element address $(M\hat{}j\ (k+1) + \Sigma_{l=0\ldots(j-1)}(M\hat{}l))$, in which M, j, k, and l are all unsigned integers; and
(b) means for connecting from the neighboring register of each of all the memory elements whose element address is $(M\hat{}j\ (k+1) + \Sigma_{l=0\ldots(j-1)}(M\hat{}l))$ to a unique input of

the register multiplexer of the memory element whose element address ($M^j k + \Sigma_{l=0...(j-1)}(M^l)$), in which M, j, k, and l are all unsigned integers.

[c88] An apparatus of claim 80, further comprising:

(a) the concurrent bus further carrying a datum to each of all the memory elements; and

(b) means for connecting the datum of the concurrent bus to a unique input of the register multiplexer of each of all the memory elements.

[c89] An apparatus of claim 80, further comprising:

(a) the concurrent bus further carrying a write selection code to each of all the memory elements;

(b) each of all the memory elements further comprising:

(1) a plurality of data registers, each being a register;

(2) a register demultiplexer, being a bus demultiplexer, comprising:

(A) an input;

(B) a plurality of outputs; and

(C) a selection input, which selects one of the outputs to be connected from the input;

(3) means for connecting:

(A) each of all the data registers to a unique input of the register multiplexer;

(B) each of all the data registers from a unique out-

put of the register demultiplexer;

(C) the neighboring register from a unique output of the register demultiplexer;

(D) the operation register to the input of the register demultiplexer; and

(E) the write selection code of the concurrent bus to the selection input of the register demultiplexer; and

(4) means for exclusively activating either (A) the register multiplexer, or (B) the register demultiplexer; and

(c) the concurrent means further comprising:

(1) write selecting means for selecting the same one of the outputs of the register demultiplexer of each of all the enabled memory elements; and

(2) the write means further comprising means for copying the content of the operation register to the register which has been selected by the write means.

[c90] An apparatus of claim 89, each of all its memory elements further comprising:

(a) All the registers are addressable.

[c91] Task switching steps for alternatively operating on a plurality of arrays stored in the apparatus of claim 90, the task switching steps further comprising:

(a) steps for using one set of data registers to store data for a task in each memory element which are used by the task; and

(b) while operating on the set of data registers in each memory element which are used by the task, steps for updating all other data registers in each memory element which are used by the task and all registers of the memory elements which are not used by the task.

[c92] An apparatus of claim 80, each of its memory elements further comprising:

(a) state means for defining states for the memory element when it is enabled; and

(b) conditional means for carrying out operation code on the concurrent bus when the memory element is in a required state.

[c93] An apparatus of claim 92, further comprising:

(a) each of all the memory elements further comprising:

(1) at least one status bit;

(2) means for either (A) positively or (B) negatively asserting any of the status bits; and

(3) the state means further comprising means for using the values of the status bit(s) to define the state of the memory element; and

(b) the concurrent means further comprising:

(1) status means for either (A) positively or (B) nega-

tively asserting any of the status bits of each of all the enabled memory elements.

[c94] An apparatus of claim 92, each of its memory elements further comprising:

(a) the required state being a predefined state.

[c95] An apparatus of claim 92, further comprising:

(a) the concurrent bus further carrying a condition specification to each of all the memory elements; and

(b) the conditional means further comprising:

(1) specifying means for using the condition specification of the concurrent bus to specify the required state, and

(2) determining means for determining if the state of the memory element matches the required state which has been specified by the condition specification of the concurrent bus.

[c96] An apparatus of claim 92, further comprising:

(a) each of its memory elements further comprising:

(1) an match bit output; and

(b) the concurrent means further comprising:

(1) match means for positively asserting the match bit output of each of all the enabled memory element.

[c97] An apparatus of claim 96, further comprising:

(a) a parallel counter, comprising:

(1) a plurality of bit inputs,

(2) a count output,

(3) means for concurrently counting the bit inputs which are positively asserted;

(b) means for connecting:

(1) the match bit output of each of all the memory elements to a unique bit input of the parallel counter, and

(2) the count output of the parallel counter to the input/output control unit;

(c) the concurrent means further comprising:

(1) matching means for specifying the required state for the conditional means concurrently to all the memory element by the data stored in each enabled memory element and a matching requirement; and

(2) counting means for concurrently counting the enabled memory element whose match bit outputs are positively asserted; and

(d) the instruction means further comprising:

(1) means for concurrently specifying a matching requirement to all the memory elements; and

(2) means for writing the count of the enabled memory elements each of which satisfies the matching requirement.

[c98] Steps for using the apparatus of claim 97, further comprising:

(a) steps for concurrently defining or concurrently changing the selection of the enabled memory elements for matching;

(b) steps for concurrently specifying a matching requirement to all the memory elements; and

(c) steps for concurrently counting the enabled memory elements each of which satisfies the matching requirement.

[c99] An apparatus of claim 96, further comprising:

(a) a priority encoder, comprising:

(1) a plurality of bit inputs, each of which corresponds to a unique address;

(2) a no-hit bit output, which is positively asserted when none of the bit inputs is positively asserted;

(3) a priority high bit input; and

(4) an address output, when the no-hit bit output being negatively asserted, the address output containing either (A) the highest address of the bit inputs which are positively asserted when the priority high bit input is positively asserted, or (B) the lowest address of the bit inputs which are positively asserted when the priority high bit input is negatively asserted;

(b) means for connecting:

(1) the match bit output of each of all the memory elements to a unique bit input of the priority encoder, thus each of all the memory elements having a unique address;

(2) the priority high bit input of the priority encoder from the input/output control unit; and

(3) the no-hit bit output and the address output of the priority encoder to the input/output control unit;

(c) the concurrent means further comprising:

(1) matching means for defining the required state for the conditional means concurrently to all the memory element by the data stored in each enabled memory element and a matching requirement;

(2) null means for signaling none of the enabled memory elements whose match bit output is positively asserted; and

(3) addressing means for finding either (A) the highest or (B) the lowest address of the enabled memory element whose match bit output is positively asserted; and

(d) the instruction means further comprising:

(1) means for concurrently specifying a matching requirement to all the memory elements;

(2) means for writing a predefined value to the external connection of the apparatus if no enabled mem-

ory element satisfying the matching requirement; and

(3) means for writing to the external connection of the apparatus either (A) the highest or (B) the lowest address of the enabled memory element which satisfies the matching requirement.

[c100] Steps for using the apparatus of claim 99, further comprising:

(a) steps for concurrently defining or concurrently changing the selection of the enabled memory elements for matching;

(b) steps for concurrently specifying a matching requirement to each of all the memory elements;

(c) steps for concurrently finding none of the enabled memory elements satisfying the matching requirement;

(d) steps for concurrently finding the highest address of the enabled memory elements which satisfies the matching requirement;

(e) steps for concurrently finding the lowest address of the enabled memory elements which satisfies the matching requirement; and

(f) steps for concurrently enumerating the addresses of the enabled memory elements each of which satisfies the matching requirement.

[c101] An apparatus of claim 99, further comprising:

(a) a parallel counter, comprising:

(1) a plurality of bit inputs,

(2) a count output,

(3) means for concurrently counting the bit inputs which are positively asserted;

(b) means for connecting:

(1) the match bit output of each of all the memory elements to a unique bit input of the parallel counter, and

(2) the count output of the parallel counter to the input/output control unit;

(c) the concurrent means further comprising:

(1) matching means for specifying the required state for the conditional means concurrently to all the memory element by the data stored in each enabled memory element and a matching requirement; and

(2) counting means for concurrently counting the enabled memory element whose match bit outputs are positively asserted; and

(d) the instruction means further comprising:

(1) means for concurrently specifying a matching requirement to all the memory elements; and

(2) means for writing the count of the enabled memory elements each of which satisfies the matching requirement to the external connection of the appara-

tus.

[c102] Steps for using the apparatus of claim 101, further comprising:

(a) steps for concurrently defining or concurrently changing the selection of the enabled memory elements for matching;

(b) steps for concurrently specifying a matching requirement to each of all the memory elements;

(c) steps for concurrently finding none of the enabled memory elements satisfying the matching requirement;

(d) steps for concurrently finding the highest address of the enabled memory elements which satisfies the matching requirement;

(e) steps for concurrently finding the lowest address of the enabled memory elements which satisfies the matching requirement;

(f) steps for concurrently enumerating the addresses of the enabled memory elements each of which satisfies the matching requirement; and

(g) steps for concurrently counting the enabled memory elements each of which satisfies the matching requirement.

[c103] An apparatus of claim 101, further comprising:

(a) a general decoder, comprising:

(1) a start address input;

(2) an end address input;

(3) a carry number input;

(4) a plurality of bit outputs, each of which has a unique address; and

(5) means for concurrently positively asserting all the bit outputs whose addresses are: (A) no less than the value at the start address input, (B) no more than the value at the end address input, and (C) an integer increment of the value at the carry number input starting from the value at the start address input, while negatively asserting all the other bit outputs;

(b) means for connecting each of all the memory elements to the bit output of the general decoder which has the same address as the memory element;

(c) the input/output control unit further comprising:

(1) controlling means for providing the start address input, the end address input, and the carry number input to the general decoder; and

(d) the enabling means further comprising:

(1) means for positively asserting the enable bit inputs of the memory elements whose element addresses are: (A) no less than a start address, (B) no more than an end address, and (C) an integer increment of a carry number starting from the start address.

[c104] An apparatus of claim 103, further comprising:

(a) dividing means for obtaining (A) the quotient, and (B) the value of dividend minus reminder, of dividing a dividend by a divider, the dividend being the value of a subtrahend minus an offset, the dividing means further comprising:

(1) means for inputting the offset into the start address input of the general decoder;

(2) means for inputting the subtrahend to the end address input of the general decoder;

(3) means for inputting the divider to the carry number input of the general decoder;

(4) means for connecting each of all bit outputs of the general decoder to a unique bit input of the parallel counter, except the bit output at address 0 of the general decoder;

(5) means for outputting the quotient from the count output of the parallel counter;

(6) means for connecting each of all bit outputs of the general decoder to the bit input which has same address of the priority encoder, except (A) the bit output at address 0 of the general decoder, and (B) negatively asserting the bit input at address 0 of the priority encoder;

(7) means for positively asserting the priority high bit input of the priority encoder;

(8) when the no-hit bit output of the priority encoder is positively asserted, means for signaling the divider being 0; and

(9) when the no-hit bit output of the priority encoder is negatively asserted, means for outputting the value of dividend minus reminder from the address output of the priority encoder; and

(b) the instruction means further comprising:

(1) means for obtaining (A) the quotient, and (B) the value of dividend minus reminder, of dividing a dividend by a divider, the dividend being the value of a subtrahend minus an offset.

[c105] An apparatus of claim 104, further comprising:

(a) a plurality of bit storage elements;

(b) means for connecting:

(1) each enable bit input of all the memory elements from a unique bit storage element; and

(2) each of all the bit storage element from a unique bit output of the general decoder;

(c) saving means for saving the value of each of all the bit outputs of the general decoder to the corresponding bit storage element; and

(d) retaining means for retaining the value of the bit storage elements when obtaining (A) the quotient, and (B) the value of dividend minus reminder, of dividing a

dividend by a divider, the dividend being the value of a subtrahend minus an offset.

[c106] An apparatus of claim 92, each of all the memory elements further comprising:

(a) a value comparator, comprising:

(1) a first input;

(2) a second input;

(3) an equal bit output, which is positively asserted when the value of the first input equals the value of the second input; and

(4) a larger bit output, which is either (A) positively asserted when the value at the first input is larger than the value at the second input, or (B) negatively asserted when the value at the first input is smaller than the value at the second input;

(b) means for connecting:

(1) the output of the register multiplexer to the first input of the value comparator; and

(2) the operation register to the second input of the value comparator; and

(c) the state means further comprising means for using (A) the equal bit output of the value comparator and (B) the larger bit output of the value comparator to define the state of the memory element.

[c107] An apparatus of claim 106, each of its memory elements further comprising:

(a) the value comparator being a parallel comparator, comprising:

(1) a first input;

(2) a second input;

(3) an equal bit output;

(4) a larger bit output; and

(5) means for concurrently comparing the value at the first input and the value at the second input so that: (A) the equal bit output is positively asserted when the value at the first input is equal to the value at the second input; (B) the larger bit output is positively asserted when the value at the first input is larger than the value at the second input; and (C) the larger bit output is negatively asserted when the value at the first input is smaller than the value at the second input.

[c108] An apparatus of claim 106, further comprising:

(a) each of all the memory elements further comprising:

(1) at least one status bit;

(2) means for either (A) positively or (B) negatively asserting any of the status bits; and

(3) the state means further comprising means for using the values of the status bit(s) to define the state

of the memory element; and

(b) the concurrent means further comprising:

(1) status means for either (A) positively or (B) negatively asserting any of the status bits of each of all the enabled memory elements.

[c109] An apparatus of claim 106, further comprising:

(a) each of its memory elements further comprising:

(1) an match bit output; and

(b) the concurrent means further comprising:

(1) match means for positively asserting the match bit output of each of all the enabled memory element.

[c110] An apparatus of claim 106, further comprising:

(a) the concurrent bus further carrying a datum to each of all the memory elements; and

(b) means for connecting the datum of the concurrent bus to a unique input of the register multiplexer of each of all the memory elements.

[c111] An apparatus of claim 106, further comprising:

(a) the concurrent bus further carrying a write selection code to each of all the memory elements;

(b) each of all the memory elements further comprising:

(1) a plurality of data registers, each being a register;

(2) a register demultiplexer, being a bus demulti-

plexer, comprising:

(A) an input;

(B) a plurality of outputs; and

(C) a selection input, which selects one of the outputs to be connected from the input;

(3) means for connecting:

(A) each of all the data registers to a unique input of the register multiplexer;

(B) each of all the data registers from a unique output of the register demultiplexer;

(C) the neighboring register from a unique output of the register demultiplexer;

(D) the operation register to the input of the register demultiplexer; and

(E) the write selection code of the concurrent bus to the selection input of the register demultiplexer;

(4) means for exclusively activating either (A) the register multiplexer, or (B) the register demultiplexer; and

(c) the concurrent means further comprising:

(1) write selecting means for selecting the same output of the register demultiplexer of each of all the enabled memory elements; and

(2) the write means further comprising means for

copying the content of the operation register to the register which has been selected by the write selection means.

[c112] An apparatus of claim 106, further comprising:

(a) the concurrent bus further carrying a condition code to each of all the memory elements;

(b) each of all the memory elements further comprising:

(1) a control unit, comprising:

(A) an operation code input;

(B) executing means for executing an operation code at the operation code input;

(C) an condition code input;

(D) determining means for determining if the state of the memory element matches the required state which has been specified by an condition code at the condition code input; and

(E) conditional means for carrying out the executing means when the memory element is in the required state; and

(2) means for connecting:

(A) the operation code of the concurrent bus to the control unit;

(B) the condition code of the concurrent bus to the control unit; and

(C) the larger bit output and the equal bit output of the value comparator to the control unit; and

(c) the concurrent means further comprising:

(1) specifying means for using the condition code of the concurrent bus to specify the required state for the conditional means, and

(2) determining means for determining if the state of each of all the enabled memory elements matches the required state which has been specified by the condition code of the concurrent bus.

[c113] An apparatus of claim 112, further comprising:

(a) the concurrent bus further carrying to each of all the memory elements:

(1) a datum; and

(2) a write selection code;

(b) each of all the memory elements further comprising:

(1) at least one status bit;

(2) status means for either (A) positively or (B) negatively asserting any of the status bits;

(3) means for connecting the status bit with the control unit;

(4) the state means further comprising means for using the values of the status bits to define the state of the memory element;

(5) a match bit output;

(6) a plurality of data registers, each being a register;

(7) a register demultiplexer, being a bus demultiplexer, comprising:

(A) an input;

(B) a plurality of outputs; and

(C) a selection input, which selects one of the outputs to be connected from the input;

(8) means for connecting:

(A) the datum of the concurrent bus to a unique input of the register multiplexer;

(B) each of all the data registers to a unique input of the register multiplexer;

(C) each of all the data registers from a unique output of the register demultiplexer;

(D) the neighboring register from a unique output of the register demultiplexer;

(E) the operation register to the input of the register demultiplexer; and

(F) the write selection code of the concurrent bus to the selection input of the register demultiplexer; and

(9) means for exclusively activating either (A) the register multiplexer, or (B) the register demultiplexer; and

(c) the concurrent means father comprising:

(1) status means for either (A) positively or (B) negatively asserting any of the status bits of each of all the enabled memory elements; and

(2) match means for positively asserting the match bit output of each of all the enabled memory element;

(3) write selecting means for selecting the same output of the register demultiplexer of each of all the enabled memory elements; and

(4) the write means further comprising means for copying the content of the operation register to the register which has been selected by the write selection means.

[c114] An apparatus of claim 113, its instructing means further comprising means for instructing each of its memory elements in the general format of "condition: operation register", in which:

(a) the "register" specifies (A) the read selection code, and (B) the write selection code, which can be any one of:

(1) the datum of the concurrent bus;

(2) the neighboring register of the memory element itself;

(3) the neighboring register of the memory element whose element address is immediately lower than the

element address of the memory element itself;

(4) the neighboring register of the memory element whose element address is immediately higher than the element address of the memory element itself; and

(5) any one of the data registers;

(b) the "condition" specifies the condition code for the conditional means, which can be any one from the following set:

(1) the value relation between the operation register and the output of the register multiplexer, comprising any one of: (A) smaller, (B) smaller or equal, (C) equal, (D) not equal, (E) larger or equal, and (F) larger;

(2) the value of any of the status bits, comprising either (A) positively asserted, or (B) negatively asserted;

(3) the AND combination of (1) and (2); and

(4) the OR combination of (1) and (2);

(c) the "operation" specifies the operation code, comprising:

(1) read means for copying the content of the register specified by "register" to the operation register;

(2) write means for copying the content of the operation register to the register specified by "register" other than the neighboring registers of the neighboring memory elements;

(3) status means for asserting any of the status bits; and

(4) match means for asserting the match bit output of the element.

[c115] An apparatus of claim 114, each of all its memory elements further comprising:

(a) a first and a second OR gates, each comprising:

(1) a plurality of bit inputs; and

(2) a bit output, which is positively asserted when any of the bit inputs is positively asserted;

(b) a first and a second AND gates, each comprising:

(1) a plurality of bit inputs; and

(2) a bit output, which is positively asserted when all of the bit inputs are positively asserted;

(c) means for connecting:

(1) each bit of the output of the register multiplexer to a unique bit input of the first OR gate;

(2) the bit output of the first OR gate to the control unit;

(3) each bit of the output of the register multiplexer to a unique bit input of the first AND gate;

(4) the bit output of the first AND gate to the control unit;

(5) each bit of the output of the operation register to a unique bit input of the second OR gate;

(6) the bit output of the second OR gate to the control unit;

(7) each bit of the output of the operation register to a unique bit input of the second AND gate; and

(8) the bit output of the second AND gate to the control unit;

(d) the "condition" code for the instruction means comprising any one of the following set:

(1) the value relation between the operation register and the output of the register multiplexer, comprising any one of: (A) smaller, (B) smaller or equal, (C) equal, (D) not equal, (E) larger or equal, and (F) larger;

(2) the value of any of the status bits, comprising any one of: (A) positively asserted, and (B) negatively asserted;

(3) either (A) the AND or (B) the OR combination of all the bit of the output from the register multiplexer;

(4) either (A) the AND or (B) the OR combination of all the bit of the output from the operation register;

(5) the AND combination of (1) and (2);

(6) the OR combination of (1) and (2);

(7) the AND combination of (1) and (3);

(8) the OR combination of (1) and (3);

(9) the AND combination of (1) and (4);

(10) the OR combination of (1) and (4);

(11) the AND combination of (2) and (3);

(12) the OR combination of (2) and (3);

(13) the AND combination of (2) and (4);

(14) the OR combination of (2) and (4);

(15) the AND combination of (3) and (4); and

(16) the OR combination of (3) and (4);

[c116] An apparatus of claim 113, further comprising:

(a) a parallel counter, comprising:

(1) a plurality of bit inputs,

(2) a count output,

(3) means for concurrently counting the bit inputs which are positively asserted;

(b) a priority encoder, comprising:

(1) a plurality of bit inputs, each of which corresponds to a unique address;

(2) a no-hit bit output, which is positively asserted when none of the bit inputs is positively asserted;

(3) a priority high bit input; and

(4) an address output, when the no-hit bit output being negatively asserted, the address output containing either (A) the highest address of the bit inputs which are positively asserted when the priority high bit input is positively asserted, or (B) the lowest address of the bit inputs which are positively asserted when the priority high bit input is negatively

asserted;

(c) means for connecting:

(1) the match bit output of each of all the memory elements to a unique bit input of the parallel counter;

(2) the count output of the parallel counter to the input/output control unit;

(3) the match bit output of each of all the memory elements to a unique bit input of the priority encoder, thus each of all the memory elements having a unique address;

(4) the priority high bit input of the priority encoder from the input/output control unit; and

(5) the no-hit bit output and the address output of the priority encoder to the input/output control unit;

(d) the concurrent means further comprising:

(1) matching means for defining the required state for the conditional means concurrently to all the memory element by the data stored in each enabled memory element and a matching requirement;

(2) counting means for concurrently counting the enabled memory elements whose match bit outputs are positively asserted;

(3) null means for signaling none of the enabled memory elements whose match bit output is positively asserted; and

(4) addressing means for finding either (A) the high-

est or (B) the lowest element address among the enabled memory elements whose match bit outputs are positively asserted; and

(e) the instruction means further comprising:

(1) means for concurrently specifying a matching requirement to each of all the memory elements;

(2) means for writing to the external connection of the apparatus the count of the enabled memory elements each of which satisfies the matching requirement;

(3) means for writing a predefined value to the external connection of the apparatus if no enabled memory element satisfying the matching requirement; and

(4) means for writing to the external connection of the apparatus either (A) the highest or (B) the lowest address among those of the enabled memory elements each of which satisfies the matching requirement.

[c117] Steps for using the apparatus of claim 116, further comprising:

(a) steps for concurrently defining or concurrently changing the selection of the enabled memory elements for matching;

(b) steps for concurrently specifying specifying a re-

quirement for the conditional means to each of all the memory elements;

(c) steps for storing an array by the apparatus;

(d) steps for concurrently finding none of the array item satisfying the matching requirement;

(e) steps for concurrently finding the highest address of the array item which satisfies the matching requirement;

(f) steps for concurrently finding the lowest address of the array item which satisfies the matching requirement;

(g) steps for concurrently enumerating addresses of the array items each of which satisfies the matching requirement;

(h) steps for concurrently counting the array items each of which satisfies the matching requirement;

(i) steps for concurrently constructing a histogram of the array;

(j) steps for concurrently finding the local extreme values of the array;

(k) steps for concurrently finding a global limit of the array;

(l) steps for concurrently finding a global extreme value of the array;

(m) steps for concurrently sorting the array;

(n) steps for concurrently inserting a new array item anywhere in the array;

(o) steps for concurrently deleting a existing array item

anywhere in the array; and

(p) steps for concurrently exchanging two existing array items anywhere in the array.

[c118] An apparatus of claim 116, it connecting means further comprising:

(a) means for connecting from the neighboring register of each of all the memory elements whose element address is $(M\hat{}j\ k + \Sigma_{l=0\ldots(j-1)}(M\hat{}l))$ to a unique input of the register multiplexer of the memory element whose element address is $(M\hat{}j\ (k+1) + \Sigma_{l=0\ldots(j-1)}(M\hat{}l))$, in which M, j, k and l are all unsigned integers; and

(b) means for connecting from the neighboring register of each of all the memory elements whose element address is $(M\hat{}j\ (k+1) + \Sigma_{l=0\ldots(j-1)}(M\hat{}l))$ to a unique input of the register multiplexer of the memory element whose element address is $(M\hat{}j\ k + \Sigma_{l=0\ldots(j-1)}(M\hat{}l))$, in which M, j, k and l are all unsigned integers.

[c119] An apparatus of claim 118, in which M equals to 3.

[c120] Steps for using the apparatus of claim 119, further comprising:

(a) steps for concurrently defining or concurrently changing the selection of the enabled memory elements for matching;

(b) steps for concurrently specifying a requirement for

the conditional means to each of all the memory elements;

(c) steps for storing an array by the apparatus;

(d) steps for concurrently sampling the array items;

(e) steps for concurrently finding the global limit of the array; and

(f) steps for concurrently sorting the array.

[c121] An apparatus of claim 116, further comprising:

(a) each of all its memory elements further comprising:

(1) means for incrementing the operation register;

(b) the concurrent means father comprising:

(1) incrementing means for incrementing the operation register of each of all the enabled memory elements.

[c122] Steps for using the apparatus of claim 121, further comprising:

(a) steps for concurrently defining or concurrently changing the selection of the enabled memory elements for matching;

(b) steps for concurrently specifying a requirement for the conditional means to each of all the memory elements;

(c) steps for storing an array by the apparatus;

(d) steps for concurrently finding none of the array item satisfying the requirement;

(e) steps for concurrently finding the highest address among the array item each of which satisfies the requirement;

(f) steps for concurrently finding the lowest address of the array item which satisfies the requirement;

(g) steps for concurrently enumerating addresses of the array items each of which satisfies the requirement;

(h) steps for concurrently counting the array items each of which satisfies the requirement;

(i) steps for concurrently constructing a histogram of the array;

(j) steps for concurrently finding the degree of matching each of all the array item against the requirement;

(k) steps for concurrently finding the local extreme values of the array;

(l) steps for concurrently finding the local extreme values of the array with a difference threshold;

(m) steps for concurrently finding a global limit of the array;

(n) steps for concurrently finding a global extreme value of the array;

(o) steps for concurrently sorting the array;

(p) steps for concurrently inserting a new array item anywhere in the array;

(q) steps for concurrently deleting a existing array item anywhere in the array; and

(r) steps for concurrently exchanging two existing array items anywhere in the array.

[c123] An apparatus of claim 113, each of all its memory elements further comprising:

(a) a carry bit, being a status bit;

(b) an adder, comprising:

(1) a first input;

(2) a second input;

(3) a carry bit input;

(4) a sum output, which holds the sum value of adding the values of the carry bit input, the first input, and the second input; and

(5) a carry bit output, which holds the carry bit value of adding the values of the carry bit input, the first input, and the second input;

(c) a operation multiplexer, being a bus multiplexer, comprising:

(1) a plurality of inputs;

(2) an output; and

(3) a selection input, which selects one of the inputs to the output;

(d) means for connecting:

(1) the carry bit to the carry bit input of the adder;

(2) the carry bit from the carry bit output of the adder;

(3) the output of the register multiplexer to the first input of the adder;

(4) the operation register to the second input of the adder;

(5) the sum output of the adder to a unique input of the operation multiplexer;

(6) the output of the register multiplexer to a unique input of the operation multiplexer;

(7) the output of the operation multiplexer to the operation register; and

(8) the selection input of the operation multiplexer from the operation code of the concurrent bus; and

(e) the concurrent means means further comprising:

(1) carry means for setting a value of either (A) 0 or (B) 1 to the carry bit; and

(2) adding means for adding the values of (A) the carry bit, (B) the output of the register multiplexer, and (C) the operation register, and means for saving the result at (A) the carry bit, and (B) the operation register.

[c124] An apparatus of claim 123, the adder in each of all its memory elements being a parallel adder, further comprising:

(a) adding means for concurrently adding the values of (A) the carry bit, (B) the output of the register multi-

plexer, and (C) the operation register, and means for saving the result at (A) the carry bit, and (B) the operation register.

[c125] An apparatus of claim 124, further comprising:

(a) the adder parallel in each of all its memory elements further comprising:

(1) an AND output;

(2) means for outputting to the AND output, the result of bitwise AND combining the values of the first input and the second input;

(3) an OR output;

(4) means for outputting to the OR output, the result of bitwise OR combining the values of the first input and the second input;

(5) a XOR output; and

(6) means for outputting to the XOR output, the result of bitwise XOR combining the values of the first input and the second input;

(b) means for connecting:

(1) the AND output of the parallel adder to a unique input of the operation multiplexer;

(2) the OR output of the parallel adder to a unique input of the operation multiplexer; and

(3) the XOR output of the parallel adder to a unique input of the operation multiplexer;

(c) the concurrent means further comprising:

(1) AND means for bitwise logically AND combining the values of (A) the operation register, and (B) the register specified by the read selection code, and means for copying the result to the operation register;

(2) OR means for bitwise logically OR combining the values of (A) the operation register, and (B) the register specified by the read selection code, and means for copying the result to the operation register; and

(3) XOR means for bitwise logically XOR combining the values of (A) the operation register, and (B) the register specified by the read selection code, and means for copying the result to the operation register.

[c126] An apparatus of claim 123, further comprising:

(a) each of all its memory elements further comprising:

(1) means for logically bitwise inverting the output from the register multiplexer;

(2) means for connecting the logically bitwise inversion of the output from the register multiplexer into a unique input of the operation multiplexer; and

(b) the instructing means further comprising:

(1) inverting means for bitwise logically inverting the value of the register specified by the read selection

code, and means for copying the result to the operation register.

[c127] An apparatus of claim 126, further comprising:

(a) each of all its memory elements further comprising:

(1) an adder multiplexer, being a bus multiplexer, comprising:

(A) a first input and a second input;

(B) an output; and

(C) a selection bit input, which selects either the first input or the second input to the output;

(2) means for connecting:

(A) the output from the register multiplexer to the first input of the adder multiplexer;

(B) the logically bitwise inversion of the output from the register multiplexer to the second input of the adder multiplexer;

(C) the output from the adder multiplexer into the first input of the adder; and

(D) the selection bit input of the adder multiplexer from the operation code of the concurrent bus;

(b) the instructing means further comprising:

(1) subtracting means for subtracting (A) the value of the register specified by the read selection code, from (B) the value of the operation register, and

means for copying the result to the operation register.

[c128] An apparatus of claim 123, further comprising:

(a) each of all its memory elements further comprising:

(1) means for logically bitwise inverting the operation register; and

(2) means for connecting the logically bitwise inversion of the operation register into a unique input of the operation multiplexer;

(b) the instructing means further comprising:

(1) inverting means for bitwise logically inverting the value of the operation register, and means for copying the result to the operation register; and

(2) subtracting means for subtracting (A) the value of the operation register, from (B) the value of the register specified by the read selection code, and means for copying the result to the operation register.

[c129] Steps for using the apparatus of claim 123, further comprising:

(a) steps for concurrently defining or concurrently changing the selection of the enabled memory elements for operating upon;

(b) steps for concurrently specifying a requirement for the conditional means to each of all the memory elements;

(c) steps for storing an array by the apparatus;
(d) steps for concurrently finding none of the array item satisfying the requirement;
(e) steps for concurrently finding the highest address among the array item each of which satisfies the requirement;
(f) steps for concurrently finding the lowest address of the array item which satisfies the requirement;
(g steps for concurrently enumerating addresses of the array items each of which satisfies the requirement;
(h) steps for concurrently counting the array items each of which satisfies the requirement;
(i) steps for concurrently constructing a histogram of the array;
(j) steps for concurrently finding the degree of matching each of all the array item against the requirement;
(k) steps for concurrently finding the local extreme values of the array;
(l) steps for concurrently finding the local extreme values of the array with a difference threshold;
(m) steps for concurrently finding a global limit of the array;
(n) steps for concurrently finding a global extreme value of the array;
(o) steps for concurrently sorting the array;
(p) steps for concurrently inserting a new array item any-

where in the array;

(q) steps for concurrently deleting a existing array item anywhere in the array; and

(r) steps for concurrently exchanging two existing array items anywhere in the array.

(s) steps for concurrently carrying out a local operation involve neighboring array items;

(t) steps for concurrently finding the sum of neighboring array items; and

(u) steps for concurrently matching a template against neighboring array items of the array.

[c130] An apparatus of claim 123, further comprising:

(a) a X general decoder and a Y general decoder, each comprising:

(1) a start address input;

(2) an end address input;

(3) a carry number input;

(4) a plurality of bit outputs, each of which has a unique address; and

(5) means for concurrently positively asserting all the bit outputs whose addresses are: (A) no less than the value at the start address input, (B) no more than the value at the end address input, and (C) an integer increment of the value at the carry number input starting from the value at the start address input, while

negatively asserting all the other bit outputs;

(b) means for connecting:

(1) each of all the memory elements to a unique bit output of the X general decoder, thus each of all the memory elements having a unique X address; and

(2) each of all the memory elements to a unique bit output of the Y general decoder, thus each of all the memory elements having a unique Y address;

(c) the input/output control unit further comprising:

(1) controlling means for providing (A) the X start address input, (B) the X end address input, and (C) the X carry number input to the X general decoder; and

(2) controlling means for providing (A) the Y start address input, (B) the Y end address input, and (C) the Y carry number input to the Y general decoder;

(d) the enabling means further comprising means for positively asserting the enable bit inputs of the memory elements:

(1) whose X addresses are: (A) no less than the X start address, (B) no more than the X end address, and (C) an integer increment of the X carry number starting from the X start address; and

(2) whose Y addresses are: (A) no less than the Y start address, (B) no more than the Y end address, and (C) an integer increment of the Y carry number starting from the X start address;

(e) the neighboring means further comprising:

(1) left connecting means for connecting from the neighboring register of each of all the memory elements to a unique inputs of the register multiplexer of the memory element which has immediately lower X address but same Y address;

(2) right connecting means for connecting from the neighboring register of each of all the memory elements to a unique input of the register multiplexer of the memory element which has immediately higher X address but same Y address;

(3) bottom connecting means for connecting from the neighboring register of each of all the memory elements to a unique inputs of the register multiplexer of the memory element which has immediately lower Y address but same X address; and

(4) top connecting means for connecting from the neighboring register of each of all the memory elements to a unique input of the register multiplexer of the memory element which has immediately higher Y address but same X address.

[c131] Steps for using the apparatus of claim 130, further comprising:

(a) steps for concurrently defining or concurrently changing the selection of the enabled memory elements

for operating upon;

(b) steps for concurrently specifying a requirement for the conditional means to each of all the memory elements;

(c) steps for storing an array by the apparatus;

(d) steps for concurrently finding none of the array item satisfying the requirement;

(e) steps for concurrently finding the highest address among the array item each of which satisfies the requirement;

(f) steps for concurrently finding the lowest address of the array item which satisfies the requirement;

(g) steps for concurrently enumerating addresses of the array items each of which satisfies the requirement;

(h) steps for concurrently counting the array items each of which satisfies the requirement;

(i) steps for concurrently constructing a histogram of the array;

(j) steps for concurrently finding the degree of matching each of all the array item against the requirement;

(k) steps for concurrently finding the local extreme values of the array;

(l) steps for concurrently finding the local extreme values of the array with a difference threshold;

(m) steps for concurrently finding a global limit of the array;

(n) steps for concurrently finding a global extreme value of the array;

(o) steps for concurrently sorting the array;

(p) steps for concurrently inserting a new array item anywhere in the array;

(q) steps for concurrently deleting a existing array item anywhere in the array; and

(r) steps for concurrently exchanging two existing array items anywhere in the array.

(s) steps for concurrently carrying out a local operation involve neighboring array items;

(t) steps for concurrently finding the sum of neighboring array items;

(u) steps for concurrently matching a template against neighboring array items of the array;

(v) steps for concurrently detecting all lines at the atan(Mx / My) direction on an image, in which Mx and My are both integer; and

(w) steps for concurrently detecting all lines at all directions on an image.

[c132] An apparatus of claim 113, further comprising:

(a) the concurrent bus further carrying to each of all the memory elements:

(1) a bit read selection code; and

(2) a bit write selection code;

(b) each of all its memory elements further comprising:

(1) the register multiplexer and a bit multiplexer, each being a multi-channel multiplexer further comprising:

(A) an address input;

(B) a plurality of bit inputs, each of which corresponds to a unique input address at the address input;

(C) a width input;

(D) a plurality of bit outputs, each of which corresponds to a unique output address at the width input; and

(E) connecting means for connecting each bit input of input address (A + j) to the bit output of output address j, in which A is the value at the address input and j is between 0 and (W - 1), in which W is the value at the width input, while negatively asserting all the other bit outputs;

(2) a register demultiplexer and a bit demultiplexer, each being a multi-channel demultiplexer further comprising:

(A) an address input;

(B) a plurality of bit outputs, each of which corresponds to an output address at the address input;

(C) a width input;

(D) a plurality of bit inputs, each of which corresponds to an input address at the width input; and

(E) connecting means for connecting each bit input of input address j to the bit output of output address (A + j), in which A is the value at the address input and j is between 0 and (W - 1), in which W is the value at the width input, while negatively asserting all the other bit outputs;

(3) means for connecting:

(A) the read selection code of the concurrent bus to the address input of the register multiplexer;

(B) the write selection code of the concurrent bus to the address input of the register demultiplexer;

(C) the bit read selection code of the concurrent bus to the address input of the bit multiplexer;

(D) the bit write selection code of the concurrent bus to the address input of the bit demultiplexer;

(E) each bit of the datum of the concurrent bus to a unique bit input of the register multiplexer;

(F) each bit of each of all the data registers to a unique bit input of the register multiplexer;

(G) each bit of each of all the data registers from a

unique bit output of the register demultiplexer;

(H) each bit of the neighboring register to a unique bit input of the register multiplexer;

(I) each bit of the neighboring register from a unique bit output of the register demultiplexer;

(J) each bit of the operation register to a unique bit input of the bit multiplexer;

(K) each bit of the operation register from a unique bit output of the bit demultiplexer;

(L) the output of the register multiplexer to the input of the bit demultiplexer;

(M) the output of the bit multiplexer to the input of the register demultiplexer;

(N) the output of the register multiplexer to the first input of the value comparator;

(O) the output of the bit multiplexer to the second input of the value comparator; and

(4) means for exclusively activating either (A) the register multiplexer and the bit multiplexer, or (B) the register demultiplexer and the bit demultiplexer; and

(c) the neighboring means further comprising:

(1) means for connecting from each bit of the neighboring register of each of all the memory elements to

a unique bit input of the register multiplexer of each of the memory elements which have immediately adjacent addresses.

[c133] An apparatus of claim 132, each of all its memory elements further comprising:

(a) a carry bit, being a status bit;

(b) an adder, comprising:

(1) a first input;

(2) a second input;

(3) a carry bit input;

(4) a sum output, which holds the sum value of adding the values of the carry bit input, the first input, and the second input; and

(5) a carry bit output, which holds the carry bit value of adding the values of the carry bit input, the first input, and the second input;

(c) a operation multiplexer, being a bus multiplexer, comprising:

(1) a plurality of inputs;

(2) an output; and

(3) a selection input, which selects one of the inputs to the output;

(d) means for connecting:

(1) the carry bit to the carry bit input of the adder;

(2) the carry bit from the carry bit output of the

adder;

(3) the output of the register multiplexer to the first input of the adder;

(4) the output of the bit multiplexer to the second input of the adder;

(5) the sum output of the adder to a unique input of the operation multiplexer;

(6) the output of the register multiplexer to a unique input of the operation multiplexer;

(7) the output of the operation multiplexer to the input of the bit demultiplexer; and

(8) the selection input of the operation multiplexer from the operation code of the concurrent bus; and

(e) the concurrent means means further comprising:

(1) carry means for setting a value of either (A) 0 or (B) 1 to the carry bit; and

(2) adding means for adding the values of (A) the carry bit, (B) the bit section of the register specified by the read selection code, and (C) the bit section of the operation register specified by the bit read selection code, and means for saving the result at (A) the carry bit, and (B) the bit section of the operation register specified by the bit write selection code.

[c134] An apparatus of claim 132, its instructing means further comprising means for instructing each of its memory el-

ements in the general format of "condition: operation wide [bit] register[bit]", in which:

(a) the "width" specifies the value at (A) the width input of the bit multiplexer, (B) the width input of the bit demultiplexer, (C) the width input of the register multiplexer, and (D) the width input of the register demultiplexer;

(b) the "register[bit]" specifies (A) the read selection code, and (B) the write selection code, in which "register" can be any one of:

(1) the datum on the concurrent bus;

(2) the neighboring register of the memory element itself;

(3) the neighboring register of any of the memory elements which have immediately adjacent addresses than the address of the memory element itself; and

(4) any one of the data registers;

(c) the "[bit]" specifies (A) the bit read selection code, and (B) the bit write selection code;

(d) the "condition" specifies the condition code for the conditional means; and

(e) the "operation" specifies the operation code.

[c135] Steps for using the apparatus of claim 133, further comprising:

(a) steps for concurrently defining or concurrently

changing the selection of the enabled memory elements for operating upon;

(b) steps for concurrently specifying a requirement for the concurrent means to each of all the memory elements;

(c) steps for concurrently shifting the bit section specified by the read selection code by a value in each of all the enabled memory elements;

(d) steps for concurrently shifting the bit section specified by the bit read selection code by a value in each of all the enabled memory elements;

(e) steps for concurrently obtaining the sum of the register specified by the read selection code and the operation register in each of all the enabled memory elements;

(f) steps for concurrently obtaining the difference of the register specified by the read selection code and the operation register in each of all the enabled memory elements;

(g) steps for concurrently obtaining the production of the register specified by the read selection code and the operation register in each of all the enabled memory elements;

(h) steps for concurrently obtaining the division of the register specified by the read selection code and the operation register in each of all the enabled memory elements; and

(i) steps for concurrently carrying out generic mathematical operations.

[c136] An all-line decoder, which is an apparatus, comprising:

(a) an address input;

(b) a plurality of bit outputs, each of which corresponds to a unique address at the address input; and

(c) activating means for concurrently positively asserting all the bit outputs whose address are equal to or less than the address input while negatively asserting all the other bit outputs, the activating means further comprising:

(1) the address input being A = (A[N-1] ... A[0]), in which A[j] denotes the jth significant bit of the address input A of bit width N,

(2) the bit output being F[A, N], in which A denotes the corresponding address A of the bit output and N denotes the bit width of the address input A, and

(3) means for building an all-line-decoder with address bit input width of (N + 1) from an all-line-decoder with address bit input width of N using the logic expression of F[A, N]:

F[0, 1] = 1;

F[1, 1] = A[0];

F[(0 A[N-1] ... A[0]), N+1] = F[(A[N-1] ... A[0]), N] + A[N];

F[(1 A[N-1] ... A[0]), N+1] = F[(A[N-1] ... A[0]), N] A[N].

[c137] An apparatus of claim 136, further comprising:

(a) an enable bit input; and

(b) disabling means for signaling the values of all the outputs of the apparatus being invalid for the current input values when the enable bit input is negatively asserted.

[c138] A carry patent generator, which is an apparatus, comprising:

(a) a carry number input, inputting a carry number being an unsigned integer;

(b) a plurality of bit outputs, each of which having a unique address; and

(c) activating means for positively asserting all the bit outputs whose addresses are an integer-fold of the carry number while negatively asserting all the other bit outputs, the activating means further comprising:

(1) the address for each of all the bit outputs being A = (A[N-1] ... A[0]), in which A[j] denotes the jth significant bit of the address A of bit width N;

(2) C(A) being the binary expression of the value of the address A;

(3) all possible values of the carry number forming a

set C;

(4) the natural number factors of the value of the address A forming a set Q(A);

(5) the set K(A) being the overlap set between set C and set Q(A), with a unique element of the set K(A) denoted as K(A)[k]; and

(6) means for generating the bit output F[A] as:

$F[0] = 1;$

IF $A \in K(A)$: $F[A] = \Sigma_k D[K(A)[k]] + C[A];$

ELSE: $F[A] = \Sigma_k D[K(A)[k]]$

[c139] An apparatus of claim 138, further comprising:

(a) an enable bit input; and

(b) disabling means for signaling the values of all the outputs of the apparatus being invalid for the current input values when the enable bit input is negatively asserted.

[c140] An apparatus of claim 138, further comprising:

(a) means for implementing the carry pattern generator using a standard two-layer OR-AND logic, so that the implementation of the carry pattern generator can be extended easily to accommodate additional bits of the carry number input.

[c141] A parallel left shifter, which is an apparatus, comprising:

(a) a plurality of bit inputs, each of which having a

unique address;

(b) a plurality of bit outputs, each of which corresponding to a unique bit input, thus to the corresponding address as well;

(c) a shift amount input, inputting a shift amount being a unsigned integer; and

(d) connecting means for concurrently connecting each of all the bit inputs to the bit output whose address equals the sum of the address of the bit input and the value of the shift amount input while negatively asserting all the other bit outputs, the connecting means further comprising:

(1) the shift amount input being S = (S[N-1] ... S[0]), in which S[j] denotes the jth significant bit of the shift amount input S of bit width N;

(2) N count of switching layers, with the bit output from each switching layer being F[A, j+1], in which A is the address of the bit output, and j denote any one of the switch layers, and

(3) switching means for concurrently switching F[A, j+1] by any one of the switching layers according to the logic expression:

S[j] == 0: F[A, j+1] = F[A, j];

S[j] == 1 AND A > 2^j: F[A, j+1] = F[A-2^j, j];

S[j] == 1 AND A <= 2^j: F[A, j+1] = 0.

[c142] An apparatus of claim 141, further comprising:

(a) an enable bit input; and

(b) disabling means for signaling the values of all the outputs of the apparatus being invalid for the current input values when the enable bit input is negatively asserted.

[c143] A parallel right shifter, which is an apparatus, comprising:

(a) a plurality of bit inputs, each of which having a unique address;

(b) a plurality of bit outputs, each of which corresponding to a unique bit input, thus to the corresponding address as well;

(c) a shift amount input, inputting a shift amount being a unsigned integer; and

(d) connecting means for concurrently connecting each of all the bit outputs to the bit input whose address equals the sum of the address of the bit output and the value of the shift amount input while negatively asserting all the other bit outputs, the connecting means further comprising:

(1) the shift amount input being S = (S[N-1] ... S[0]), in which S[j] denotes the jth significant bit of the shift amount input S of bit width N;

(2) N count of switching layers, with the bit output

from each switching layer being F[A, j+1], in which A is the address of the bit output, and j denote any one of the switch layers, and

(3) switching means for concurrently switching F[A, j+1] by any one of the switching layers according to the logic expression:

S[j] == 0: F[A, j+1] = F[A, j];

S[j] == 1 AND A > 2^j: F[A - 2^j, j+1] = F[A, j];

S[j] == 1 AND A <= 2^j: F[A, j+1] = 0.

[c144] An apparatus of claim 143, further comprising:

(a) an enable bit input; and

(b) disabling means for signaling the values of all the outputs of the apparatus being invalid for the current input values when the enable bit input is negatively asserted.

[c145] A range decoder, which is an apparatus, comprising:

(a) a start address input;

(b) an end address input;

(c) a plurality of bit outputs, each of which has a unique address; and

(e) decoding means for concurrently positively asserting all the bit outputs whose addresses are: (A) no less than the value at the start address input, and (B) no more than the value at the end address input, while negatively as-

serting all the other bit outputs; the decoding means further comprising:

(1) a first and a second all-line decoder, each of which comprises:

(A) an address input,

(B) a plurality of bit outputs, each of which corresponds to a unique address at the address input, and

(C) means for concurrently positively asserting all the bit outputs whose address are equal to or less than the address input while negatively asserting all the other bit outputs;

(2) means for connecting:

(A) the start address input of the range decoder to the address input of the first all-line decoder,

(B) the end address input of the range decoder to the address input of the second all-line decoder,

(C) each of all the bit outputs of the range decoder from the logic-AND combination of: (A) the logical inversion of the bit output of the first all-line decoder which has the same address, and (B) the bit output of the second all-line decoder which has the same address.

[c146] An apparatus of claim145, further comprising:

(a) an enable bit input; and

(b) disabling means for signaling the values of all the outputs of the apparatus being invalid for the current input values when the enable bit input is negatively asserted.

[c147] A general decoder, which is an apparatus, comprising:

(a) a start address input;

(b) an end address input;

(c) a carry number input;

(d) a plurality of bit outputs, each of which has a unique address; and

(e) decoding means for concurrently positively asserting all the bit outputs whose addresses are: (A) no less than the value at the start address input, (B) no more than the value at the end address input, and (C) an integer increment of the value at the carry number input starting from the value at the start address input, while negatively asserting all the other bit outputs, the decoding means further comprising:

(1) a carry patent generator, comprising:

(A) a carry number input, the carry number being an unsigned integer;

(B) a plurality of bit outputs, each of which corresponds to a unique bit output address which is one

of the zero-based one-incremental consecutive values; and

(C) means for positively asserting all the bit outputs each of whose addresses is an integer-fold of the carry number while negatively asserting all the other bit outputs;

(2) a parallel left shifter, comprising:

(A) a plurality of bit inputs, each having a unique address,

(B) a plurality of bit outputs, each of which corresponds to a unique bit input, thus to the corresponding unique address as well,

(C) a shift amount input, inputting an unsigned integer, and

(D) means for connecting each of all the bit inputs to the bit output whose address equals the sum of the address of the bit input and the value of the shift amount input while negatively asserting all the other bit outputs;

(3) an all-line decoder, comprising:

(A) an address input,

(B) a plurality of bit outputs, each of which corresponds to a unique address at the address input,

and

(C) means for concurrently positively asserting all the bit outputs whose address are equal to or less than the address input while negatively asserting all the other bit outputs;

(4) means for connecting:

(A) the carry number input of the general decoder to the carry number input of the carry pattern generator,

(B) the start address input of the general decoder to the shift amount input of the parallel left shifter,

(C) the end address input of the general decoder to the address input of the all-line decoder,

(D) each of all the bit outputs of the carry pattern generator to the bit input of the parallel left shifter which has the same address,

(E) each of all the element control bit outputs of the general decoder from the logic-AND combination of: (A) the bit output of the parallel left shifter which has the same address, and (B) the bit output of the all-line decoder which has the same address.

[c148] An apparatus of claim147, further comprising:

(a) an enable bit input; and

(b) disabling means for signaling the values of all the outputs of the apparatus being invalid for the current input values when the enable bit input is negatively asserted.

[c149] A parallel divider, which is an apparatus, comprising:

(a) a dividend input;

(b) a divider input;

(c) a quotient output;

(d) a largest output;

(e) an exception bit output, which signaling the value of the divider input being 0; and

(f) dividing means for obtaining (A) the quotient at the quotient output, and (B) the value of dividend minus reminder at the largest output, of dividing the dividend at the dividend input by the divider at the divider input, the dividing means further comprising:

(1) an all-line decoder, comprising:

(A) an address input,

(B) a plurality of bit outputs, each of which corresponds to a unique address at the address input, and

(C) means for concurrently positively asserting all the bit outputs whose address are equal to or less than the address input while negatively asserting

all the other bit outputs;

(2) a carry patent generator, comprising:

(A) a carry number input, the carry number being an unsigned integer;

(B) a plurality of bit outputs, each of which corresponds to a unique address; and

(C) means for positively asserting all the bit outputs whose addresses are an integer-fold of the carry number while negatively asserting all the other bit outputs;

(3) a high-priority encoder, comprising:

(A) a plurality of bit inputs, each of which corresponds to a unique address;

(B) a no-hit bit output, which is positively asserted when none of the bit inputs is positively asserted; and

(C) an address output, which contains the highest address of the bit inputs which are positively asserted when the no-hit bit output is negatively asserted;

(4) a parallel counter, comprising:

(A) a plurality of bit inputs,

(B) a count output,

(C) means for concurrently counting the bit inputs which are positively asserted;

(5) means for connecting:

(A) the dividend input to the address input of the all-line decoder;

(B) the divider input to the carry number input of the carry pattern generator;

(C) except the bit input at address 0, each of all the bit inputs of the high-priority encoder from the logic-AND combination of: (A) the bit output of the carry pattern generator which has the same address, and (B) the bit output of the all-line decoder which has the same address, while negatively asserting the bit input at address 0 of the high-priority encoder;

(D) each of all the bit inputs of the high-priority encoder to an unique bit input of the parallel counter, except the bit input at address 0 of the high-priority encoder;

(E) the quotient output from the count output of the parallel counter;

(F) the largest output from the address output of the high-priority encoder; and

(G) the exception bit output from the no-hit bit output of the high-priority encoder.

[c150] An apparatus of claim 149, further comprising:
(a) an enable bit input;
(b) disabling means for signaling the values of all the outputs of the apparatus being invalid for the current input values when the enable bit input is negatively asserted.

[c151] A parallel comparator, which is an apparatus, comprising:
(a) a first input;
(b) a second input;
(c) an equal bit output;
(d) a larger bit output; and
(e) comparing means for concurrently comparing the value at the first input and the value at the second input so that: (A) the equal bit output is positively asserted when the value at the first input is equal to the value at the second input; (B) the larger bit output is positively asserted when the value at the first input is larger than the value at the second input; and (C) the larger bit output is negatively asserted when the value at the first input is smaller than the value at the second input; the comparing means further comprising:

(1) the first input being X = (X[N-1] ... X[0]), in which X[j] denotes the jth significant bit of the first input X of bit width N,

(2) the second input being Y = (Y[N-1] ... Y[0]), in which Y[j] denotes the jth significant bit of the second input Y of bit width N,

(3) the corresponding bits of X and Y being concurrently and independently compared to obtain G and L, as:

G[j] = X[j] !Y[j];

L[j] = !X[j] Y[j];

(4) the corresponding bits of G and L being concurrently and independently OR combined to Z, as:

Z[j] = G[j] + L[j];

(5) each of all the bits of Z being connected to the input bit of a high-priority encoder with the bit's significance in Z being the same as the input bit's address of the encoder, the address at the address output of the encoder thus containing the most significance of the bit at where X and Y differs, and the no-hit bit output of the high-priority encoder, which is the equal bit output of the parallel comparator, being positively asserted when X and Y are equal, and

(6) the address output of the high-priority encoder being connected to the address input of a multi-

plexer, which each of all the bits of G being connected to the input bit of the multiplexer with the bit's significance in G being the same as the input bit's address, so that the bit output of the multiplexer, which is the larger bit output of the parallel comparator, is positively asserted when X is larger than Y, and negatively asserted when X is smaller than Y.

[c152] An apparatus of claim 151, further comprising:

(a) an enable bit input;

(b) disabling means for signaling the values of all the outputs of the apparatus being invalid for the current input values when the enable bit input is negatively asserted.

[c153] A parallel adder, which is an apparatus, comprising:

(a) a carry bit input;

(b) a first input;

(c) a second input;

(d) a sum output; and

(e) adding means for outputting to the sum output, the sum of the values of the carry bit input, the first input and the second input, the adding means further comprising:

(1) the carry bit input being C[0];

(2) the first input being X = (X[N-1] ... X[0]), in which

X[j] denotes the jth significant bit of the first input X of bit width N;

(3) the second input being Y = (Y[N−1] ... Y[0]), in which Y[j] denotes the jth significant bit of the second input Y of bit width N;

(4) the sum output being S = (S[N] S[N−1] ... S[0]), in which S[j] denotes the jth significant bit of the output S of bit width (N+1);

(5) means for concurrently generating bitwise carry C for X and Y:

$$C[j+1] = X[j]\ Y[j];$$

(6) means for concurrently generating bitwise sum Z for X and Y:

$$Z[j] = (X[j] + Y[j])\ !(X[j]\ Y[j]);$$

(7) means for concurrently generating carry look-ahead at jth bit:

$$A[j, n] = C[j-n]\ \Pi_{k=1 \text{ to } n}(Z[j-k]);$$

$$A[j] = \Sigma_{n=1 \text{ to } j}\ A[j, n];$$

(8) means for concurrently adding the bitwise sum Z, the bitwise carry C, and the look-ahead carry A into S:

$$S[0] = !Z[0]\ C[0] + Z[0]\ !C[0];$$

$$S[N] = C[N] + A[N];$$

$$S[j] = !Z[j]\ C[j] + Z[j]\ !C[j]\ !A[j] + !Z[j]\ A[j].$$

[c154] An apparatus of claim 153, further comprising:

(a) an AND output;

(b) means for concurrently outputting to the AND output, the result of bitwise AND combining the values of the first input and the second input;

(c) an OR output;

(d) means for concurrently outputting to the OR output, the result of bitwise OR combining the values of the first input and the second input;

(e) a XOR output; and

(f) means for concurrently outputting to the XOR output, the result of bitwise XOR combining the values of the first input and the second input.

[c155] An apparatus of claim 153, further comprising:

(a) the lock ahead logic being implemented by transmission gate logic.

[c156] An apparatus of claim 153, further comprising:

(a) an enable bit input;

(b) disabling means for signaling the values of all the outputs of the apparatus being invalid for the current input values when the enable bit input is negatively asserted.

[c157] A parallel counter, which is an apparatus, comprising:

(a) a plurality of bit inputs,

(b) a count output,

(c) counting means for concurrently counting the bit inputs which are positively asserted at the count output.

[c158] An apparatus of claim 157, further comprising:

(a) an enable bit input;

(b) disabling means for signaling the values of all the outputs of the apparatus being invalid for the current input values when the enable bit input is negatively asserted.

[c159] An apparatus of claim 157, its counting means further comprising:

(a) means for dividing the 2^N bit inputs into bit input pairs;

(b) means for adding the two bit inputs in each of all the bit input pairs by a 1-bit adder which outputs two count bits;

(c) means for building a binary tree of parallel adders of N layers, with each jth layer of all the layers comprising 2^(N-j) number of j-bit parallel adders, each of which inputs two unique j-bit outputs from the (j-1)th layer, and generate the sum at it (j+1)-bit output; and

(d) means for connecting the output from the sole N-bit parallel adder to the counter output.

[c160] The apparatus of claim 157, the parallel adder of each

M-bit of all further comprising:

(a) a first input of M-bit;

(b) a second input of M-bit;

(c) an output of (M+1)-bit;

(d) adding means for outputting to the sum output, the sum of the values of the first input and the second input, the adding means further comprising:

(1) the first input being X = (X[M-1] ... X[0]), in which X[j] denotes the jth significant bit of the first input X of bit width M;

(2) the second input being Y = (Y[M-1] ... Y[0]), in which Y[j] denotes the jth significant bit of the second input Y of bit width M;

(3) the sum output being S = (S[M] S[M-1] ... S[0]), in which S[j] denotes the jth significant bit of the output S of bit width (M+1);

(4) means for concurrently generating bitwise carry C for X and Y:

$$C[j+1] = X[j]\ Y[j];$$

(5) means for concurrently generating bitwise sum Z for X and Y:

$$Z[j] = (X[j] + Y[j])\ !(X[j]\ Y[j]);$$

(6) means for concurrently generating carry look-ahead at jth bit when M > j > 0:

$$A[j, n] = C[j-n]\ \Pi_{k=1 \text{ to } n}(Z[j-k]);$$

$A[j] = \Sigma_{n=1 \text{ to } j} A[j, n]$;

(7) means for concurrently adding the bitwise sum Z, the bitwise carry C, and the look-ahead carry A into S:

$S[0] = [0]$

$S[1] = !Z[1]\ C[1] + Z[1]\ !C[1]$;

$S[M] = X[M-1]\ Y[M-1]$;

$S[j] = !Z[j]\ C[j] + Z[j]\ !C[j]\ !A[j] + !Z[j]\ A[j]$.

[c161] An apparatus of claim 160, further comprising:

(a) the look-ahead logic being implemented by transmission gate logic.

[c162] An apparatus of claim 157, its counting means further comprising:

(a) means for connecting each bit input to a resistor of a constant value, to product current of one constant magnitude if the bit is positively asserted, or no current if the bit is negatively asserted;

(b) means for concurrently summing the produced currents of all the bits and converting the current sum into a voltage signal by an analog op-amp, and

(c) means for using a fast analog-to-digital converter to convert the voltage signal to the count output, with a conversion scale such that each positively asserted bit input results in a cumulative one at the count output.

[c163] An apparatus of claim 157, its counting means further comprising:

(a) the bit inputs comprising (2^(2N) -1) bit inputs, in which N is a positive integer;

(b) the count output comprising (2N) bit;

(c) a plurality of smaller parallel counters, each comprising:

(1) the bit inputs comprising (2^(N) -1) bit inputs;

(2) the count output comprising N bit;

(d) a 1-bit adder, comprising:

(1) a first bit input;

(2) a second bit input;

(3) a carry bit output, which is positively asserted when both the first input and the second input are positively asserted; and

(4) a sum bit output, which is positively asserted when the first input and the second input contain different values;

(e) means for connecting the bit inputs of (2^N + 1) smaller parallel counters to the (2^(2N) -1) bit inputs of the apparatus, which are called the 1st layer smaller parallel counters;

(f) means for connecting the jth significant digit of all the count outputs of (2^N - 1) 1st layer smaller parallel counters to a smaller parallel counter, which is called the

jth 2nd layer smaller parallel counter, in which j runs from 0 to N;

(g) means for connecting all the digits except the Nth significant digits of all the count outputs of the remaining two 1st layer smaller parallel counters to a smaller parallel counter called the lone 2nd layer smaller parallel counter, with each jth significant bit at the count outputs of the 1st layer smaller parallel counter connecting to 2^j unique bit inputs of the lone 2nd layer smaller parallel counter;

(h) means for connecting the 0th significant bit of the 0th 2nd layer smaller parallel counter to the first bit input of the 1-bit adder, the 0th significant bit of the lone 2nd layer smaller parallel counter to the second bit input of the 1-bit adder, and the sum bit output of the 1-bit adder to the 0th significant bit of the count output of the apparatus; and

(i) means for connecting each of the remaining smaller parallel counters as a 1-bit adder of multiple carry bit inputs and multiple carry bit outputs.

[c164] A multi-channel multiplexer, being an apparatus, comprising:

(a) an address input;

(b) a plurality of bit inputs, each of which corresponds to a unique input address at the address input;

(c) a width input;

(d) a plurality of bit outputs, each of which corresponds to a unique output address at the width input; and

(e) connecting means for connecting each bit input of input address (A + j) to the bit output of output address j, in which A is the value at the address input and j is between 0 and (W - 1), in which W is the value at the width input, while negatively asserting all the other bit outputs.

[c165] An apparatus of claim 164, further comprising:

(a) an enable bit input; and

(b) disabling means for signaling the values of all the outputs of the apparatus being invalid for the current input values when the enable bit input is negatively asserted.

[c166] The apparatus of claim 164 being implemented by transmission gate logic.

[c167] A multi-channel demultiplexer being an apparatus comprising:

(a) an address input;

(b) a plurality of bit outputs, each of which corresponds to an output address at the address input;

(c) a width input;

(d) a plurality of bit inputs, each of which corresponds to an input address at the width input; and

(e) connecting means for connecting each bit input of input address j to the bit output of output address (A + j), in which A is the value at the address input and j is between 0 and (W - 1), in which W is the value at the width input, while negatively asserting all the other bit outputs.

[c168] An apparatus of claim 167, further comprising:
(a) an enable bit input; and
(b) disabling means for signaling the values of all the outputs of the apparatus being invalid for the current input values when the enable bit input is negatively asserted.

[c169] The apparatus of claim 167 being implemented by transmission gate logic.